PERFECT WIRELESS EXPERIENCE

# FIBOCOM L850-GL Series

# Hardware Guide

Version: V1.1.5

Date: 2020-06-20

## Applicability Type

| No. | Product Model | Description |
|---|---|---|
| 1 | L850-GL-00 | NA |
| 2 | L850-GL-01 | NA |
| 3 | L850-GL-02 | NA |
| 4 | L850-GL-03 | NA |
| 5 | L850-GL-05 | NA |
| 6 | L850-GL-10 | L850-GL-10 series (except L850-GL-10-06) |
| 7 | L850-GL-10-06 | NA |
| 8 | L850-GL-12 | NA |
| 9 | L850-GL-20 | NA |

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## Trademark

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## Change History

| Version | Author | Date | Remark |
|---|---|---|---|
| V1.1.5 | Shu Ying | 2020-06-20 | ● Section 3.3.1, add FCPO# controlling GPIO request<br>● Section 3.4.1.2, change PEWAKE# pull high resistor to 100KΩ |
| V1.1.4 | Li Senhao | 2020-04-01 | ● Section 3.1.2, add GPIO design request<br>● Section 3.3.4, add CLKREQ# and PEWAKE# requests |
| V1.1.3 | Guan Xiangyang | 2019-12-26 | ● Section 3.3.1.2, add minimum PCIe detection time note<br>● Section 3.3.5, add timing application instruction<br>● Section 3.4.1.2, add a pull-up resistor on CLKREQ#<br>● Section 3.9, add note about the direction of MIPI signal<br>● Section 4.1.4, add RF connector assembly<br>● Section 4.5, update GNSS performance table |
| V1.1.2 | Guan Xiangyang | 2019-09-06 | Add L850-GL-20 product model |
| V1.1.1 | Guan Xiangyang | 2019-08-22 | ● Add L850-GL-10-06 and L850-GL-20 part numbers<br>● Section 2.2, list supporting RF bands of all product<br>● Section 3.4, add Chrome OS support in USB interface<br>● Section 3.3, add note of PERST# control timing in USB<br>● Section 4.3, modify LTE Band5 TX power range |
| V1.1.0 | Lei Daijun | 2019-05-05 | ● Section 3.2.3, update power consumption<br>● Section 3.3, update module control timing<br>● Section 4.5, update GNSS consumption<br>● Section 3.3.4.1, add D0 L1.2 timing<br>● Section 3.9, modify MIPI-RFFE power domain<br>● Section 5.6, update packing<br>● Section 3.4.1.2, fix Figure 3-12 abnormal display in PDF converting |
| V1.0.9 | Lei Daijun | 2018-08-06 | Add L850-GL-12 part no |
| V1.0.8 | Lei Daijun | 2018-07-13 | Modify band 30 TX power range of L850-GL-03 serial module |
| V1.0.7 | Lei Daijun | 2018-06-26 | ● Update package<br>● Add note about PERST#/CLK_REQ# 3.3V support<br>● Add antenna of B30 requirement, update power consumption and RX sensitivity |
| V1.0.6 | Lei Daijun | 2018-02-26 | ● Modify COEX pin define<br>● Delete L850-GL-02 product model |

| Version | Author | Date | Remark |
|---|---|---|---|
| V1.0.5 | Lei Daijun | 2018-01-16 | ● Modify CA combinations and TDD data throughput<br>● Modify description of power consumption condition<br>● Optimize power on/off/reset timing |
| V1.0.4 | Lei Daijun | 2017-12-06 | Update Storage and packing and PCIe signal description, power consumption, CA combine |
| V1.0.3 | Lei Daijun | 2017-07-26 | ● Update timing of power on/off and reset<br>● Update PCIe, add USB support<br>● Update power consumption, TX power, RX sensitivity and other data |
| V1.0.2 | Lei Daijun | 2017-02-09 | ● Update the content of PCIe<br>● Add the power Consumption of 3CA |
| V1.0.1 | Lei Daijun | 2016-12-16 | ● Modify the PCIe Interface Application;<br>● Update the Pin Definition: change pin65 to NC |
| V1.0.0 | Lei Daijun | 2016-12-08 | Initial version |

# Contents

# 1 Foreword

## 1.1 Introduction

The document describes the electrical characteristics, RF performance, dimensions and application environment, etc. of L850-GL (hereinafter referred to as L850). With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of L850 modules and develop products.

## 1.2 Reference Standard

The design of the product complies with the following standards:

- 3GPP TS 34.121-1 V8.11.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 34.122 V11.13.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V11.4.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit(USAT)
- 3GPP TS 36.124 V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPP TS 27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- PCI Express M.2 Specification Rev1.2

## 1.3 Related Documents

- FIBOCOM Design Guide_RF Antenna

# 2 Overview

## 2.1 Introduction

L850 is a highly integrated 4G WWAN module which uses M.2 form factor interface. It supports LTE FDD/LTE TDD/WCDMA systems and can be applied to most cellular networks of mobile carrier in the world.

## 2.2 Specification

| Specification | | |
|---|---|---|
| Operating Band | L850-GL-00, L850-GL-01, L850-GL-02, L850-GL-03, L850-GL-05, L850-GL-10 series (except L850-GL-10-06)<br>L850-GL-12<br>L850-GL-20 | LTE FDD: Band 1, 2, 3, 4, 5, 7, 8, 11, 12, 13, 17, 18, 19, 20, 21, 26, 28, 29, 30, 66 |
| | | LTE TDD: Band 38, 39, 40, 41 |
| | | WCDMA/HSPA+: Band 1, 2, 4, 5, 8 |
| | L850-GL-10-06 | LTE FDD: Band 2, 4, 5, 13 |
| GNSS | Support GPS, GLONASS, BDS | |
| LTE | 3GPP Release 11 | |
| UMTS | 3GPP Release 8 | |
| Data Transmission | LTE FDD | 450Mbps DL(Cat 9)/50Mbps UL(Cat 4) |
| | LTE TDD | 347Mbps DL(Cat 9)/30Mbps UL(Cat 4)<br>When LTE TDD achieves maximum DL rate, its UL rate can reach 10Mbps only |
| | UMTS/HSPA+ | UMTS: 384 kbps DL/384 kbps UL |
| | | DC-HSPA+: 42Mbps DL(Cat 24)/5.76Mbps UL(Cat6) |
| Power Supply | DC 3.135V~4.4V, Typical 3.3V | |
| Temperature | Normal operating temperature: -10°C~+55°C<br>Extended operating temperature: -20°C~+65°C | |
| | Storage temperature: -40°C~+85°C | |
| Physical characteristics | Interface: M.2 Key-B | |
| | Dimension：30×42×2.3mm | |
| | Weight: About 6.2 g | |

| Interface | |
|---|---|
| Antenna Connector | WWAN Main Antenna ×1 |
| | WWAN Diversity Antenna ×1 |
| Function Interface | USIM 3V/1.8V |
| | PCIe Gen1 ×1 |
| | USB 2.0 |
| | USB 3.1 Gen1 (Base on Android/Linux) |
| | W_Disable# |
| | BodySAR |
| | LED |
| | Clock |
| | Tunable antenna |
| | I2S (Reserved) |
| | I2C (Reserved) |
| **Software** | |
| Protocol Stack | IPV4/IPV6 |
| AT commands | 3GPP TS 27.007 and 27.005 |
| Firmware update | PCIe |
| Other feature | Multiple carrier |
| | Windows MBIM support |
| | Windows update |

**Note:**

When temperature goes beyond normal operating temperature range of -10°C~+55°C, RF performance of module may be slightly off 3GPP specifications. For normal operating temperature, LTE FDD Band 4 and 13 can support temperature ranging from -20° C to +60° C.

## 2.3 CA Combinations

| **CA Combinations**<br>L850-GL-00, L850-GL-01, L850-GL-02, L850-GL-03, L850-GL-05, L850-GL-10 series (except L850-GL-10-06),L850-GL-12, L850-GL-20 | | |
|---|---|---|
| 2CA | Inter-band | 1+3, 5, 8, 11, 18, 19, 20, 21, 26 |
| | | 2+4, 5, 12, 13, 17, 29, 30, 66 |
| | | 3+5, 7, 8, 19, 20, 28 |
| | | 4+5, 12, 13, 17, 29, 30 |
| | | 5+7, 30, 66 |
| | | 7+20, 28 |
| | | 8+11 |
| | | 12+30 |
| | | 13+66 |
| | | 29+30 |
| | Intra-band (non-contiguous) | 2, 3, 4, 7, 41 |
| | Intra-band (contiguous) | 2, 3, 7, 40, 41 |
| 3CA | Inter-band | 1+3+7, 1+3+8，1+3+19, 1+3+20, 1+3+28, 1+7+20, 1+7+28, 1+8+11, 1+19+21 |
| | | 2+4+5, 2+4+13, 2+5+30, 2+12+30, 2+29+30, 2+5+66, 2+13+66 |
| | | 3+7+20, 3+7+28 |
| | | 4+5+30, 4+12+30, 4+29+30 |
| | 2 intra-band (non-contiguous) plus inter-band | 2+2+5, 2+2+13 |
| | | 4+4+5, 4+4+13 |
| | 2 intra-band (contiguous) plus inter-band | 2+2+29 |
| | | 3+3+1, 3+3+5, 3+3+7, 3+3+20, 3+3+28 |
| | | 2+66+66, 5+66+66, 13+66+66 |
| | | 7+7+3, 7+7+28 |
| | Intra-band (non-contiguous) | 41, 66 |
| | Intra-band (contiguous) | 40, 41, 66 |

| CA Combinations<br>L850-GL-10-06 | | |
|---|---|---|
| 2CA | Inter-band | 2+4, 5, 13 |
| | | 4+5, 13 |
| | Intra-band (non-contiguous) | 2, 4 |
| | Intra-band (contiguous) | 2 |
| 3CA | Inter-band | 2+4+5, 2+4+13 |
| | 2 intra-band (non-contiguous) plus inter-band | 2+2+5, 2+2+13 |
| | | 4+4+5, 4+4+13 |

## 2.4 Application Framework

The peripheral applications for L850 module are shown in Figure 2-1:

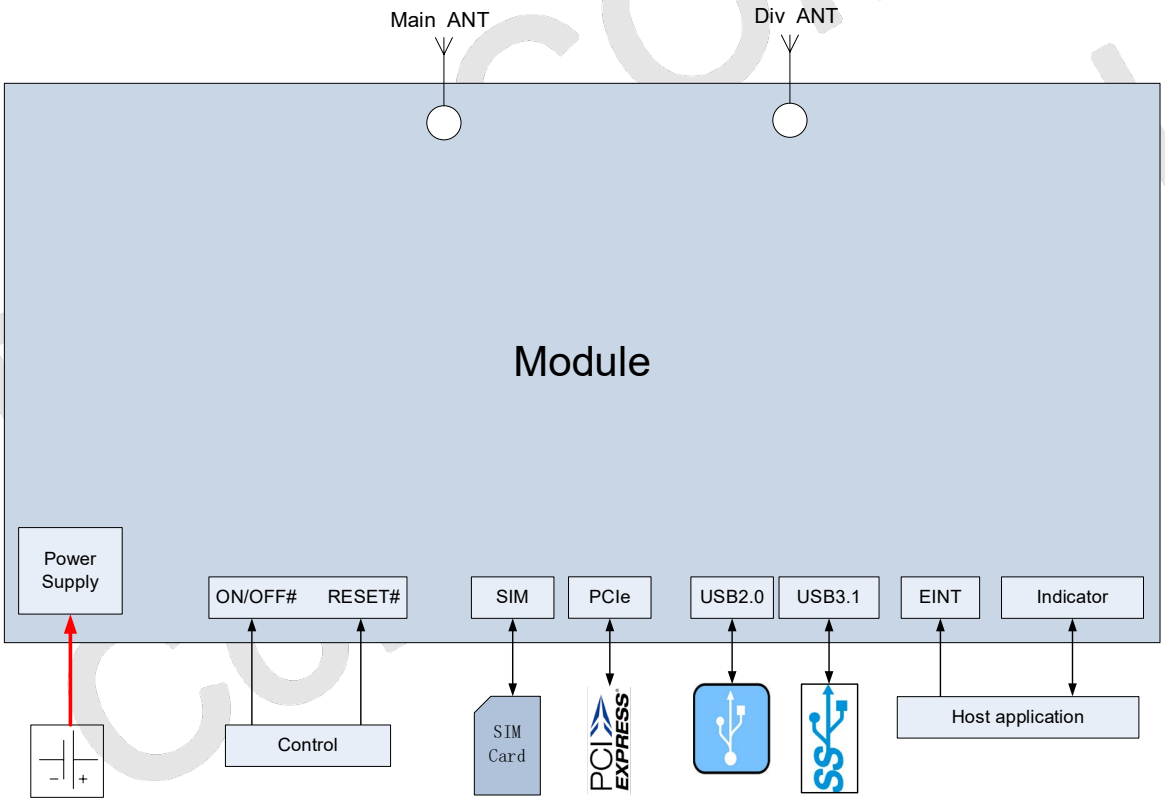


Figure2-1 Application framework

## 2.5 Hardware Block Diagram

The hardware block diagram in Figure 2-2 shows the main hardware functions of L850 module, including baseband and RF functions.

Baseband contains the followings:

- UMTS/LTE TDD/LTE FDD controller
- PMU
- NAND/internal LPDDR2 RAM
- Application interface

RF contains the followings:

- RF Transceiver
- RF Power/PA
- RF Front end
- RF Filter
- Antenna Connector

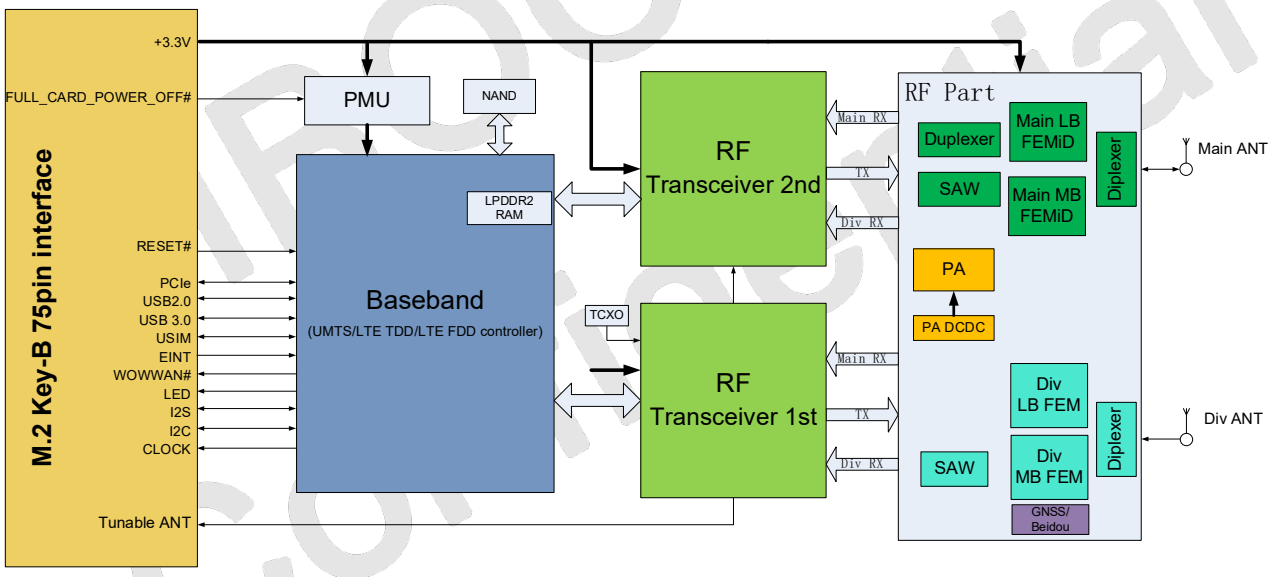


Figure 2-2 Hardware block diagram

# 3 Application Interface

## 3.1 M.2 Interface

The L850 module applies standard M.2 Key-B interface, with a total of 75 pins.

### 3.1.1 Pin Map

| | | | |
|---|---|---|---|
| 74 | +3.3V | CONFIG_2 | 75 |
| 72 | +3.3V | GND | 73 |
| 70 | +3.3V | GND | 71 |
| 68 | NC | CONFIG_1 | 69 |
| 66 | SIM_DETECT(1.8V) | RESET#(1.8V) | 67 |
| 64 | COEX_TXD(1.8V) | NC | 65 |
| 62 | COEX_RXD(1.8V) | ANTCTL2(1.8V) | 63 |
| 60 | COEX3(1.8V) | ANTCTL1(1.8V) | 61 |
| 58 | RFFE_SDATA(1.8V) | ANTCTL0(1.8V) | 59 |
| 56 | RFFE_SCLK(1.8V) | GND | 57 |
| 54 | PEWAKE# (3.3V) | REFCLKP | 55 |
| 52 | CLKREQ# (3.3V) | REFCLKN | 53 |
| 50 | PERST# (3.3V) | GND | 51 |
| 48 | TX_BLANKING(1.8V) | PERp0 | 49 |
| 46 | SYSCLK(1.8V) | PERn0 | 47 |
| 44 | GNSS_IRQ(1.8V) | GND | 45 |
| 42 | GNSS_SDA(1.8V) | PETp0 | 43 |
| 40 | GNSS_SCL(1.8V) | PETn0 | 41 |
| 38 | NC | GND | 39 |
| 36 | UIM_PWR | USB3.0_RX+ | 37 |
| 34 | UIM_DATA | USB3.0_RX- | 35 |
| 32 | UIM_CLK | GND | 33 |
| 30 | UIM_RESET | USB3.0_TX+ | 31 |
| 28 | I2S_WA(1.8V) | USB3.0_TX- | 29 |
| 26 | W_DISABLE2#(3.3/1.8V) | GND | 27 |
| 24 | I2S_TX(1.8V) | DPR(3.3/1.8V) | 25 |
| 22 | I2S_RX(1.8V) | WOWWAN#(1.8V) | 23 |
| 20 | I2S_CLK(1.8V) | CONFIG_0 | 21 |
| | Notch | Notch | |
| | Notch | Notch | |
| | Notch | Notch | |
| | Notch | Notch | |
| 10 | LED1#(3.3V OD) | GND | 11 |
| 8 | W_DISABLE1#(3.3/1.8V) | USB D- | 9 |
| 6 | FULL_CARD_POWER_OFF#(3.3/1.8V) | USB D+ | 7 |
| 4 | +3.3V | GND | 5 |
| 2 | +3.3V | GND | 3 |
| | | CONFIG_3 | 1 |

Figure 3-1 Pin map

**Note:**

Pin “Notch” represents the gap of the gold fingers.

### 3.1.2 Pin Definition

The pin definition is as follows:

| Pin | Pin Name | I/O | Reset Value | Pin Description | Type |
|---|---|---|---|---|---|
| 1 | CONFIG_3 | O | NC | NC, L850 M.2 module is configured as the WWAN – PCIe, USB3.1 interface type | - |
| 2 | +3.3V | PI | - | Power input | Power Supply |
| 3 | GND | - | - | GND | Power Supply |
| 4 | +3.3V | PI | - | Power input | Power Supply |
| 5 | GND | - | - | GND | Power Supply |
| 6 | FULL_CARD_ POWER_OFF# | I | PU | Power enable, module power on input, internal pull up | 3.3/1.8V |
| 7 | USB D+ | I/O | - | USB data plus | 0.3---3V |
| 8 | W_DISABLE1# | I | PD | WWAN disable, active low | 3.3/1.8V |
| 9 | USB D- | I/O | - | USB data minus | 0.3---3V |
| 10 | LED1# | O | T | System status LED, output open drain, 3.3V | 3.3V |
| 11 | GND | - | - | GND | Power Supply |
| 12 | Notch | | | Notch | |
| 13 | Notch | | | Notch | |
| 14 | Notch | | | Notch | |
| 15 | Notch | | | Notch | |
| 16 | Notch | | | Notch | |
| 17 | Notch | | | Notch | |
| 18 | Notch | | | Notch | |
| 19 | Notch | | | Notch | |
| 20 | I2S_CLK | O | PD | I2S serial clock, Reserved | 1.8V |
| 21 | CONFIG_0 | - | GND | GND, L850 M.2 module is configured as the WWAN – PCIe, USB3.1 interface type | - |
| 22 | I2S_RX | I | PD | I2S serial receive data, Reserved | 1.8V |

| Pin | Pin Name | I/O | Reset Value | Pin Description | Type |
|---|---|---|---|---|---|
| 23 | WOWWAN# | O | PD | Wake up host,<br>Reserved | 1.8V |
| 24 | I2S_TX | O | PD | I2S serial transmit data,<br>Reserved | 1.8V |
| 25 | DPR | I | PU | BodySAR detect, active low | 3.3/1.8V |
| 26 | W_DISABLE2# | I | PU | GNSS disable, active low,<br>Reserved | 3.3/1.8V |
| 27 | GND | - | - | GND | Power Supply |
| 28 | I2S_WA | O | PD | I2S word alignment/select,<br>Reserved | 1.8V |
| 29 | USB3.0_TX- | O | - | USB3.0 transmit data minus | - |
| 30 | UIM_RESET | O | L | SIM reset signal | 1.8V/3V |
| 31 | USB3.0_TX+ | O | - | USB3.0 transmit data plus | - |
| 32 | UIM_CLK | O | L | SIM clock signal | 1.8V/3V |
| 33 | GND | - | - | GND | Power Supply |
| 34 | UIM_DATA | I/O | L | SIM data input/output | 1.8V/3V |
| 35 | USB3.0_RX- | I | - | USB3.0 receive data minus | - |
| 36 | UIM_PWR | O | - | SIM power supply, 3V/1.8V | 1.8V/3V |
| 37 | USB3.0_RX+ | I | - | USB3.0 receive data plus | - |
| 38 | NC | - | - | NC | - |
| 39 | GND | - | - | GND | Power Supply |
| 40 | GNSS_SCL | I | PU | I2C serial clock input,<br>Reserved | 1.8V |
| 41 | PETn0 | O | - | PCIe TX differential signal<br>Negative | - |
| 42 | GNSS_SDA | I/O | PU | I2C serial data input/output,<br>Reserved | 1.8V |
| 43 | PETp0 | O | - | PCIe TX differential signal<br>Positive | - |
| 44 | GNSS_IRQ | O | PD | GNSS interrupt request output,<br>Reserved | 1.8V |
| 45 | GND | - | - | GND | Power Supply |

| Pin | Pin Name | I/O | Reset Value | Pin Description | Type |
|---|---|---|---|---|---|
| 46 | SYSCLK | O | PD | 26M clock output | 1.8V |
| 47 | PERn0 | I | - | PCIe RX differential signal Negative | - |
| 48 | TX_BLANKING | O | PD | PA blanking timer, Reserved | 1.8V |
| 49 | PERp0 | I | - | PCIe RX differential signal Positive | - |
| 50 | PERST# | I | PU | Asserted to reset module PCIe interface default. If module went into core dump, it will reset whole module, not only PCIe interface. Active low, internal pull up(10KΩ) | 3.3V |
| 51 | GND | - | - | GND | Power Supply |
| 52 | CLKREQ# | I/O | PU | Asserted by device to request a PCIe reference clock be available (active clock state) in order to transmit data. It also used by L1 PM Sub states mechanism, asserted by either host or device to initiate an L1 exit. Active low, internal pull up(10KΩ) | 3.3V |
| 53 | REFCLKN | I | - | PCIe reference clock signal, Negative | - |
| 54 | PEWAKE# | O | L | Asserted to wake up system and reactivate PCIe link from L2 to L0, it depends on system whether supports wake up functionality. Active low, open drain output and should add external pull up(100KΩ) on platform | 3.3V |
| 55 | REFCLKP | I | - | PCIe reference clock signal, Positive | - |
| 56 | RFFE_SCLK | O | - | MIPI interface tunable ANT, RFFE clock | 1.8V |
| 57 | GND | - | - | GND | Power Supply |
| 58 | RFFE_SDATA | O | - | MIPI interface tunable ANT, RFFE data | 1.8V |

| Pin | Pin Name | I/O | Reset Value | Pin Description | Type |
|---|---|---|---|---|---|
| 59 | ANTCTL0 | O | - | Tunable ANT CTRL0, bit0 | 1.8V |
| 60 | COEX3 | I/O | PD | Wireless coexistence between WWAN and WiFi/BT modules, based on BT-SIG coexistence protocol. COEX_EXT_FTA, Reserved | 1.8V |
| 61 | ANTCTL1 | O | - | Tunable ANT CTRL1, bit1 | 1.8V |
| 62 | COEX_RXD | I | T | Wireless coexistence between WWAN and WiFi/BT modules, based on BT-SIG coexistence protocol. UART receive signal(WWAN module side) Reserved | 1.8V |
| 63 | ANTCTL2 | O | - | Tunable ANT CTRL2, bit2 | 1.8V |
| 64 | COEX_TXD | O | T | Wireless coexistence between WWAN and WiFi/BT modules, based on BT-SIG coexistence protocol. UART transmit signal(WWAN module side), Reserved | 1.8V |
| 65 | NC | - | - | NC | - |
| 66 | SIM_DETECT | I | PD | SIM detect, internal pull up(390KΩ), active high | 1.8V |
| 67 | RESET# | I | - | WWAN reset input, internal pull up(10KΩ), active low | 1.8V |
| 68 | NC | - | - | NC | - |
| 69 | CONFIG_1 | O | GND | GND, L850 M.2 module is configured as the WWAN – PCIe, USB3.1 interface type | - |
| 70 | +3.3V | PI | - | Power input | Power Supply |
| 71 | GND | - | - | GND | Power Supply |
| 72 | +3.3V | PI | - | Power input | Power Supply |
| 73 | GND | - | - | GND | Power Supply |
| 74 | +3.3V | PI | - | Power input | Power Supply |
| 75 | CONFIG_2 | O | GND | GND, L850 M.2 module is configured as the WWAN – PCIe, USB3.1 interface type | - |

Reset Value: The initial status after module reset, not the status when working.

- H: High Voltage Level
- L: Low Voltage Level
- PD: Pull-Down
- PU: Pull-Up
- T: Tristate
- OD: Open Drain
- PP: Push-Pull
- PI: Power Input
- PO: Power Output

**Note:**

Digital IO pins CANNOT be connected to power directly.

The unused pins can be left floating.

All 3.3V ports are based on +3.3V power domain. When the power supply range is 3.135V~4.4V, the 3.3V ports voltage will follow the change of power supply range.

## 3.2 Power Supply

The power interface of L850 module is shown in the following table:

| Pin | Pin Name | I/O | Pin Description | DC Parameter (V) | | |
|---|---|---|---|---|---|---|
| | | | | Minimum Value | Typical Value | Maximum Value |
| 2, 4, 70, 72, 74 | +3.3V | PI | Power supply input | 3.135 | 3.3 | 4.4 |
| 36 | UIM_PWR | PO | USIM power supply | - | 1.8V/3V | - |

L850 module uses PCIe interface. According to the PCIe specification, the PCIe Vmain should be used as the +3.3V power source, not the Vaux. The Vaux is the PCIe backup power source and it is not sufficient as the power supply. In addition, the DC/DC power supply other than PCIe ports should not be used as the external power cannot control the module status through the PCIe protocol.

### 3.2.1 Power Supply

The L850 module should be powered through the +3.3V pins, and the power supply design is shown in Figure 3-2:

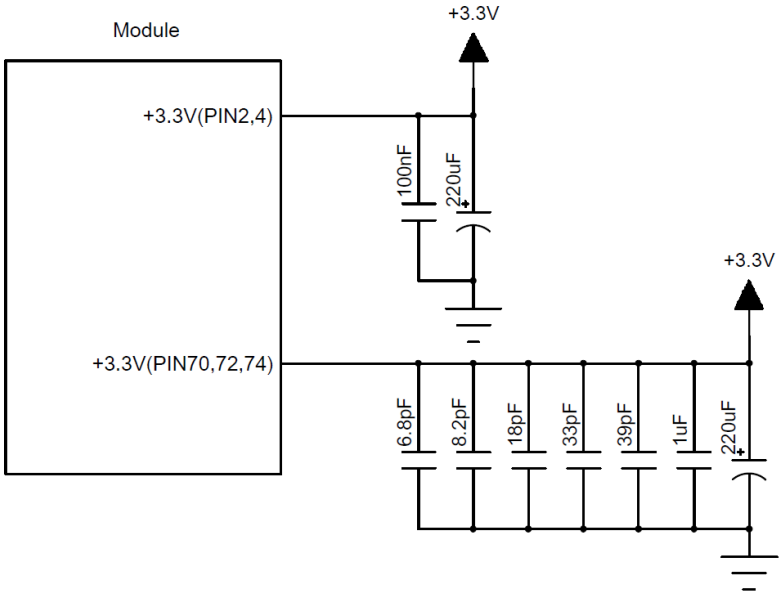


Figure 3-2 Power supply design

The filter capacitor design for power supply is shown in the following table:

| Recommended Capacitance | Application | Description |
|---|---|---|
| 220uF×2 | Voltage-stabilizing capacitors | Reduce power fluctuations of the module in operation, requiring capacitors with low ESR.<br>● LDO or DC/DC power supply requires the capacitor of no less than 440uF<br>● The capacitor for battery power supply can be reduced to 100~200uF |
| 1uF, 100nF | Digital signal noise | Filter out the interference generated from the clock and digital signals |
| 39pF, 33pF | 700/800, 850/900 MHz frequency band | Filter out low frequency band RF interference |
| 18pF, 8.2pF, 6.8pF | 1500/1700/1800/1900, 2100/2300, 2500/2600MHz frequency band | Filter out medium/high frequency band RF interference |

The stable power supply can ensure the normal operation of L850 module; and the ripple of the power supply should be less than 300mV in design. When the module operates with the maximum emission power, the maximum operating current can reach 1.5A, so the power source should be not lower than 3.135V, or the module may shut down or reboot. The power supply limits are shown in Figure 3-3:

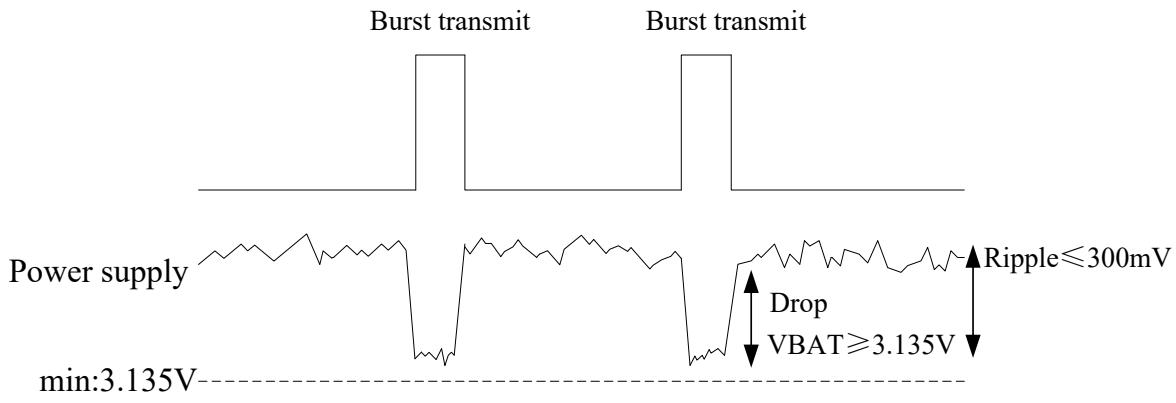


Figure 3-3 Power supply limit

### 3.2.2 Logic Level

The L850 module 1.8V logic level definition is shown in the following table:

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| 1.8V logic level | 1.71 | 1.8 | 1.89 | V |
| $V_{IH}$ | 1.3 | 1.8 | 1.89 | V |
| $V_{IL}$ | -0.3 | 0 | 0.3 | V |

The L850 module 3.3V logic level definition is shown in the following table:

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| 3.3V logic level | 3.135 | 3.3 | 3.465 | V |
| $V_{IH}$ | 2.3 | 3.3 | 3.465 | V |
| $V_{IL}$ | -0.3 | 0 | 0.3 | V |

### 3.2.3 Power Consumption

In the condition of 3.3V power supply, the L850 power consumption is shown in the following table:

| Parameter | Mode | Condition | Average Current (mA) |
|---|---|---|---|
| $I_{off}$ | Power off | Power supply, module power off | 0.05 |
| $I_{Sleep}$ | WCDMA | DRX=6 | 3.4 |
| | | DRX=8 | 2.8 |
| | | DRX=9 | 2.4 |
| | LTE FDD | Paging cycle #128 frames (1.28s DRx cycle) | 3.5 |
| | LTE TDD | Paging cycle #128 frames (1.28s DRx cycle) | 3.8 |

| Parameter | Mode | Condition | Average Current (mA) |
|---|---|---|---|
| | Radio Off | AT+CFUN=4, Flight mode | 1.8 |
| $I_{WCDMA-RMS}$ | WCDMA | WCDMA Data call Band 1 @+23.5dBm | 580 |
| | | WCDMA Data call Band 2 @+23.5dBm | 650 |
| | | WCDMA Data call Band 4 @+23.5dBm | 550 |
| | | WCDMA Data call Band 5 @+23.5dBm | 500 |
| | | WCDMA Data call Band 8 @+23.5dBm | 520 |
| $I_{LTE-RMS}$ | LTE FDD | LTE FDD Data call Band 1 @+23dBm | 700 |
| | | LTE FDD Data call Band 2 @+23dBm | 770 |
| | | LTE FDD Data call Band 3 @+23dBm | 740 |
| | | LTE FDD Data call Band 4 @+23dBm | 760 |
| | | LTE FDD Data call Band 5 @+23dBm | 560 |
| | | LTE FDD Data call Band 7 @+23dBm | 880 |
| | | LTE FDD Data call Band 8 @+23dBm | 570 |
| | | LTE FDD Data call Band 11 @+23dBm | 840 |
| | | LTE FDD Data call Band 12 @+23dBm | 640 |
| | | LTE FDD Data call Band 13 @+23dBm | 660 |
| | | LTE FDD Data call Band 17 @+23dBm | 650 |
| | | LTE FDD Data call Band 18 @+23dBm | 600 |
| | | LTE FDD Data call Band 19 @+23dBm | 550 |
| | | LTE FDD Data call Band 20 @+23dBm | 620 |
| | | LTE FDD Data call Band 21 @+23dBm | 870 |
| | | LTE FDD Data call Band 26 @+23dBm | 570 |
| | | LTE FDD Data call Band 28 @+23dBm | 580 |
| | | LTE FDD Data call Band 30 @+23dBm | 800 |
| | | LTE FDD Data call Band 66 @+23dBm | 700 |
| | LTE TDD | LTE TDD Data call Band 38 @+23dBm | 430 |

| Parameter | Mode | Condition | Average Current (mA) |
|---|---|---|---|
| | | LTE TDD Data call Band 39 @+23dBm | 340 |
| | | LTE TDD Data call Band 40 @+23dBm | 380 |
| | | LTE TDD Data call Band 41 @+23dBm | 430 |

In 3CA mode, the L850 power consumption is shown in the following table:

| 3CA Combination | Condition (Maximum Data Transfer) | Average Current (mA) |
|---|---|---|
| 1+3+7, 1+3+8，1+3+19, 1+3+20, 1+3+28, 1+7+20, 1+7+28, 1+8+11, 1+19+21<br>2+4+5, 2+4+13, 2+5+30, 2+12+30, 2+29+30<br>3+7+20, 3+7+28<br>4+5+30, 4+12+30, 4+29+30<br>5+66+2, 13+66+2<br>2+2+5, 2+2+13, 2+2+29<br>3+3+7, 3+7+7, 3+3+20<br>4+4+5, 4+4+13<br>5+66+66, 13+66+66, 66+66+2, 66+66+66<br>7+7+28, 3+3+28, 3+3+5, 1+3+3<br>40+40+40, 41+41+41 | Band 1 @+22dBm | 720 |
| | Band 2 @+22dBm | 820 |
| | Band 3 @+22dBm | 870 |
| | Band 4 @+22dBm | 820 |
| | Band 5 @+22dBm | 750 |
| | Band 7 @+22dBm | 1060 |
| | Band 8 @+22dBm | 650 |
| | Band 11 @+22dBm | 1040 |
| | Band 12 @+22dBm | 760 |
| | Band 13 @+22dBm | 760 |
| | Band 19 @+22dBm | 750 |
| | Band 20 @+22dBm | 720 |
| | Band 21 @+22dBm | 950 |
| | Band 28 @+22dBm | 670 |
| | Band 30 @+22dBm | 1160 |
| | Band 40 @+22dBm | 460 |
| | Band 41 @+22dBm | 520 |
| | Band 66 @+22dBm | 740 |

**Note：**

The data above is an average value tested on some samples at 25°C temperature.

## 3.3 Control Signal

The L850 module provides two control signals for power on/off and reset operations. The pin is defined in the following table:

| Pin | Pin Name | I/O | Reset Value | Functions | Type |
|---|---|---|---|---|---|
| 6 | FULL_CARD_POWER_OFF# | I | PU | Module power on/off input, internal pull up<br>Power on: High/Floating<br>Power off: Low | 3.3/1.8V |
| 67 | RESET# | I | - | WWAN reset input, internal pull up(10KΩ), active low | 1.8V |
| 50 | PERST# | I | PU | Asserted to reset module PCIe interface default. If module went into core dump, it will reset whole module, not only PCIe interface. Active low, internal pull up(10KΩ) | 3.3V |

**Note：**

RESET# and PERST# need to be controlled by independent GPIO, and not shared with other devices on the host. RESET# and PERST# are sensitive signals, so they should keep away from RF interference and be protected by GND. It should be neither near PCB edge nor route on surface layer to avoid module abnormal reset caused by ESD.

### 3.3.1 Module Start-Up

#### 3.3.1.1 Start-up Circuit

The FCPO# (FULL_CARD_POWER_OFF#) pin needs an external 3.3V or 1.8V pull up for booting up. AP (Application Processor) controls module start-up. The recommended design is using a default PD port to control FCPO#. It also should reserve a 100K pull down resistor on AP side. The reference design is shown in Figure3-4:

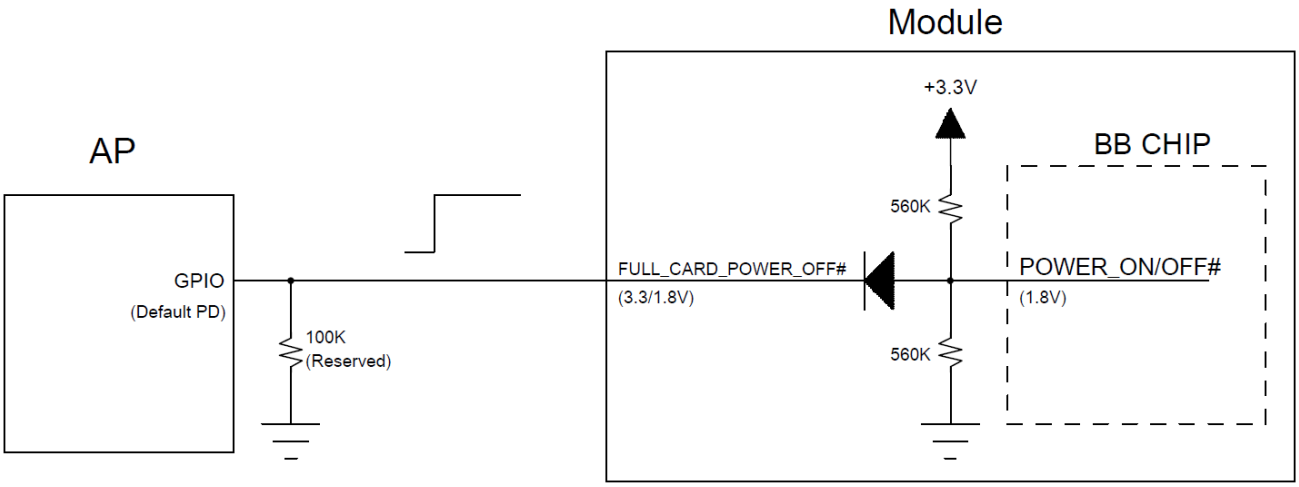


Figure 3-4 Circuit for module start-up controlled by AP

### 3.3.1.2 Start-up Timing Sequence

When power supply is ready, the PMU of module will power on and start initialization process by pulling high FCPO# signal. After about 10s, module will complete initialization process. The start-up timing is shown in Figure 3-5:

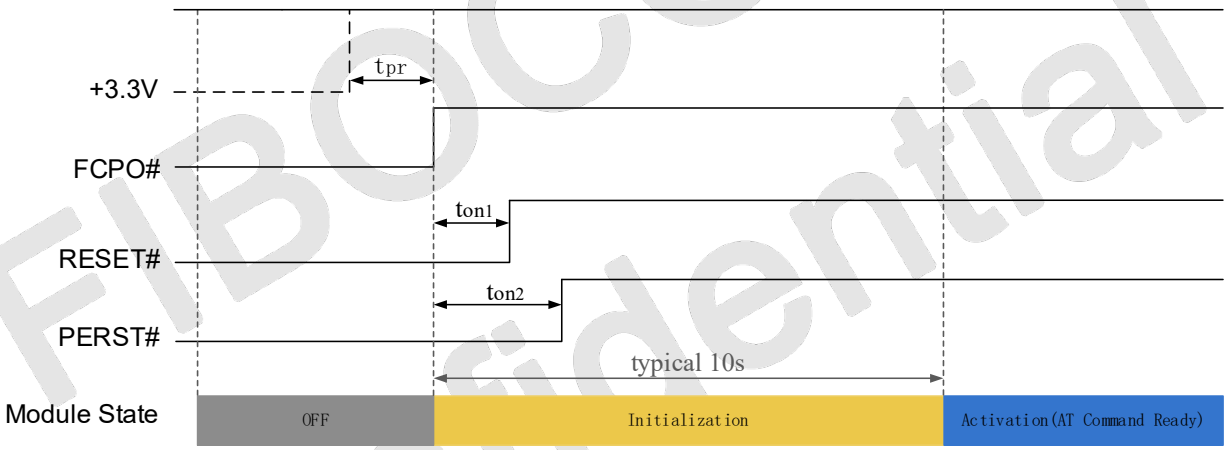


Figure 3-5 Timing control for start-up

| Index | Min. | Recommended | Max. | Comments |
|---|---|---|---|---|
| $t_{pr}$ | 0ms | - | - | The delay time of power supply rising from 0V up to 3.135V. If power supply always ready, it can be ignored |
| $t_{on1}$ | 8ms | 20ms | - | RESET# should be de-asserted after FCPO# |
| $t_{on2}$ | 50ms | 100ms | - | The time delay of PERST# de-asserted after FCPO#, PERST# must always be the last to get de-asserted |

The minimum detection time of PCIe link is about 45ms after PERST# de-asserted.

**Note：**

When USB is used as data transfer interface, follow timing above in PERST# connecting with host, otherwise don't control PERST# in PERST# floating condition.

### 3.3.2 Module Shutdown

The module can be shut down by the following controls:

| Shutdown Control | Action | Condition |
|---|---|---|
| Software | Sending AT+CFUN=0 command | Normal shutdown(recommend) |
| Hardware | Pull down FCPO# pin | Only used when a hardware exception occurs and the software control cannot be used. |

The module can be shut down by sending AT+CFUN=0 command. When the module receives the software shutdown command, the module will start the finalization process (the reverse process of initialization), and it will be completed after $t_{sd}$ time ($t_{sd}$ is the time which AP receive OK of "AT+CFUN=0", if there is no response, the max $t_{sd}$ is 5s). In the finalization process, the module will save the network, SIM card and some other parameters from memory, and then clear the memory and shut down PMU. The control timing is shown in Figure 3-6:

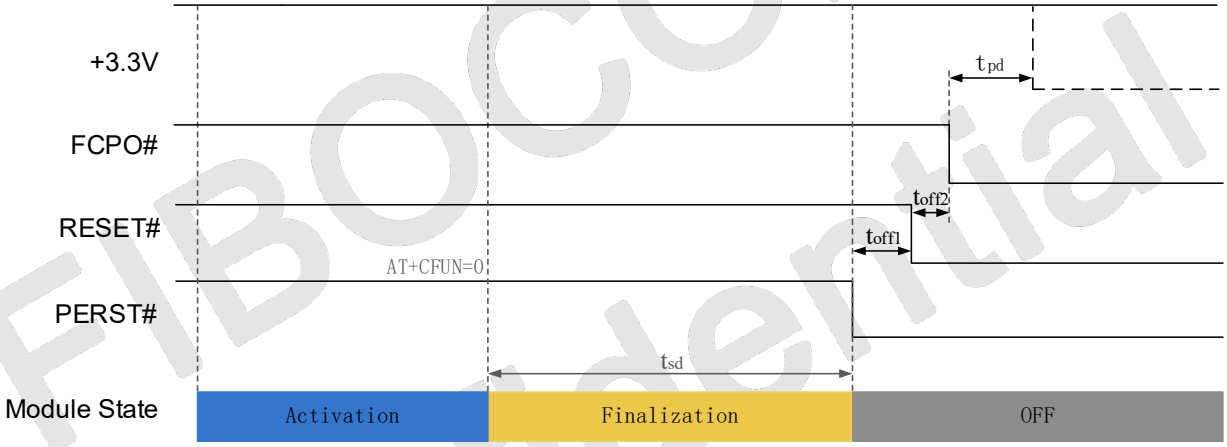


Figure 3-6 Shutdown timing control

| Index | Min. | Recommended | Max. | Comments |
|---|---|---|---|---|
| $t_{off1}$ | 16ms | 20ms | - | RESET# should be asserted after PERST# |
| $t_{off2}$ | 2ms | 10ms | - | FCPO# should be asserted after RESET# |
| $t_{pd}$ | 10ms | 100ms | - | +3.3V power supply goes down time. If power supply is always on, it can be ignored |

**Note:**

When USB is used as data transfer interface, follow timing above in PERST# connecting with host, otherwise don't control PERST# in PERST# floating condition.

### 3.3.3 Module Reset

The L850 module can reset to its initial status by pulling down the RESET# signal for more than 2ms (10ms is recommended), and module will restart after RESET# signal is released. When customer executes RESET# function, the PMU remains its power inside the module. The recommended circuit design is shown in the Figure 3-7:

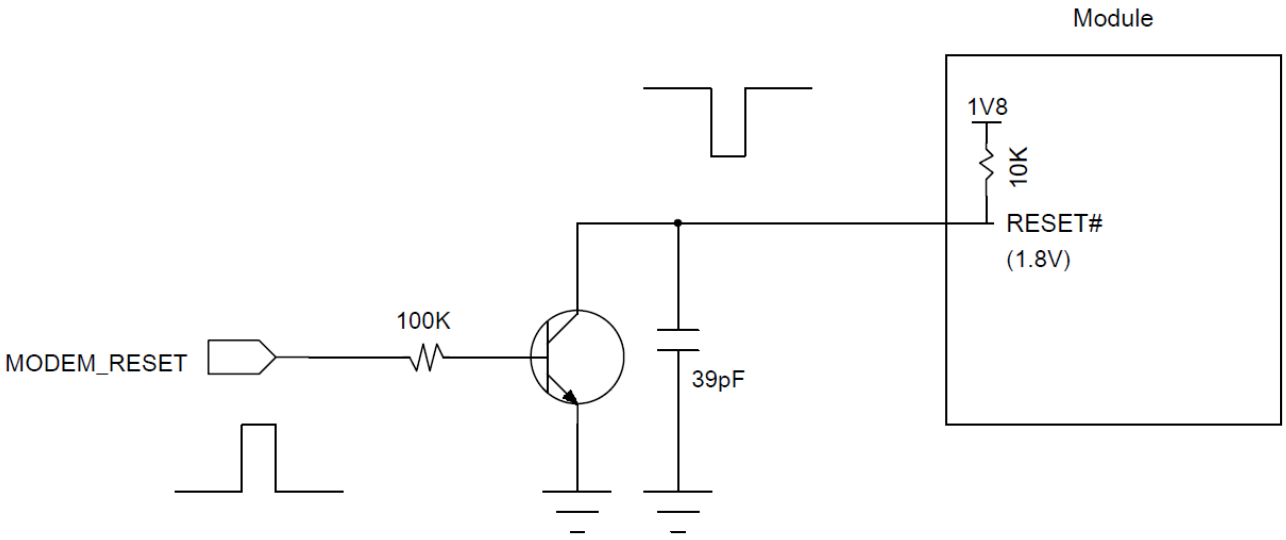


Figure 3-7 Recommended design for reset circuit

There are two reset control timings as below:

- Reset timing 1st in Figure 3-8, PMU of module internal always on in reset sequence, recommend using in FW upgrade and module recovery;
- Reset timing 2nd in Figure 3-9, PMU of module internal will be off in reset sequence (including whole power off and power on sequence, $t_{sd}$ can refer section 3.3.2), recommend using in system warm boot.

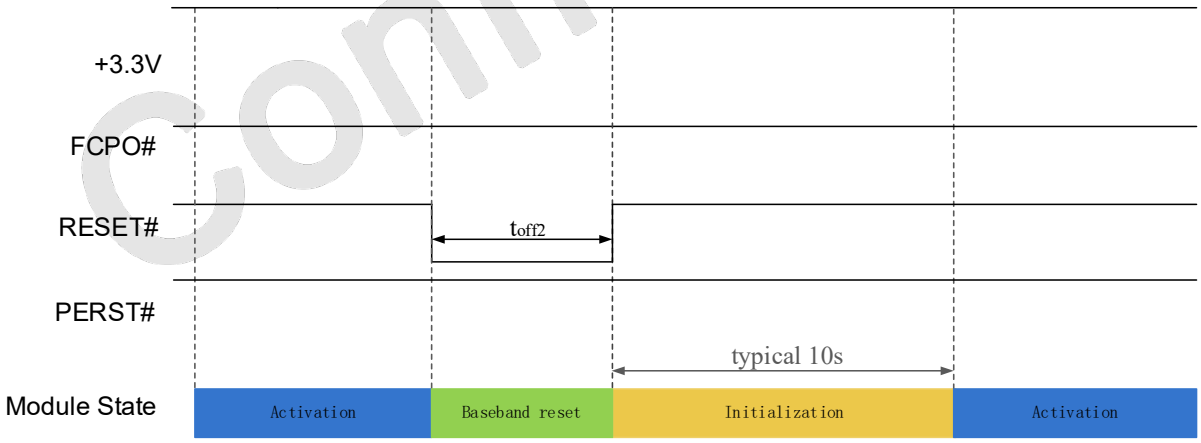


Figure 3-8 Reset timing 1st

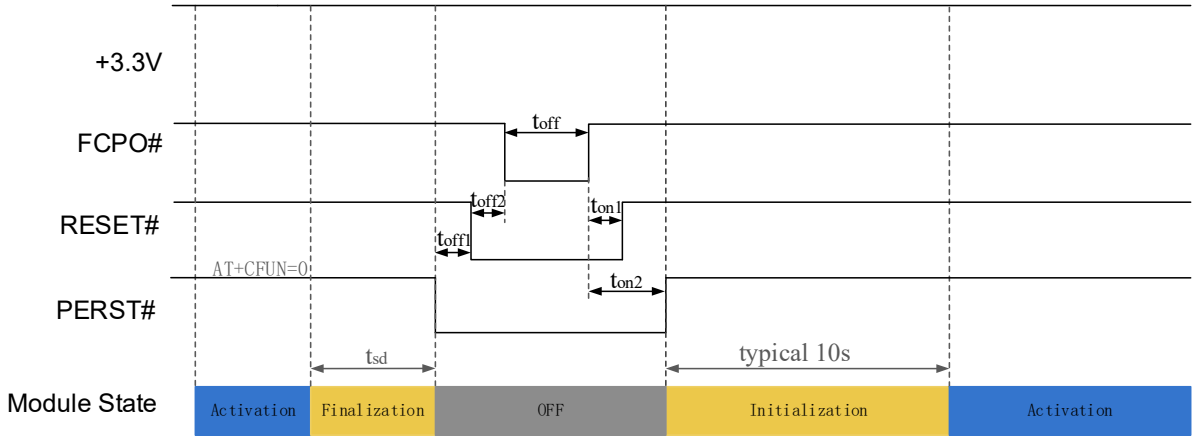


Figure 3-9 Reset timing 2nd

| Index | Min. | Recommended | Max. | Comments |
|---|---|---|---|---|
| $t_{off1}$ | 16ms | 20ms | - | RESET# should be asserted after PERST#, refer section 3.3.2 |
| $t_{off2}$ | 2ms | 10ms | - | FCPO# should be asserted after RESET#, refer section 3.3.2 |
| $t_{off}$ | 500ms | 500ms | - | Time to allow the WWAN module to fully discharge any residual voltages before the pin could be de-asserted again. This is required for both Pre-OS as well as Runtime flow |
| $t_{on1}$ | 8ms | 20ms | - | RESET# should be de-asserted after FCPO#, refer section 3.3.1.2 |
| $t_{on2}$ | 50ms | 100ms | - | The time delay of PERST# de-asserted after FCPO#, PERST# must always be the last to get de-asserted. refer section 3.3.1.2 |

**Note:**
When USB is used as data transfer interface, follow timing above in PERST# connecting with host, otherwise don't control PERST# in PERST# floating condition.

### 3.3.4 PCIe Link State

Modem has the lowest power consumption in D0 L1.2 PCIe link state. $D3_{cold}$ L2 will increase extra about 0.5mA power consumption. CLKREQ# can assert or de-assert in $D3_{cold}$ L2, but CLKREQ# shouldn't be changed again during $D3_{cold}$ L2. When CLKREQ# asserts in $D3_{cold}$ L2, it will increase extra 0.3mA power consumption compared with CLKREQ# de-asserted in $D3_{cold}$ L2. We recommend keep CLKREQ# de-asserted in $D3_{cold}$ L2.

| PCIe Link State | PERST# | CLKREQ# | Power Consumption (mA) | Description |
|---|---|---|---|---|
| D0 L1.2 | H | H | $I_{sleep}$ | Refer 3.2.3 Power Consumption |
| $D3_{cold}$ L2 | L | H | $I_{sleep}$+0.5 | The extra 0.5mA is consumed on PERST# pull down |
| | L | L | $I_{sleep}$+0.8 | The extra 0.3mA is consumed on CLKREQ# pull down |

#### 3.3.4.1 D0 L1.2

Module supports PCIe goes into D0 L1.2 state in Win10 system. The D0 L0@S0/S0ix→ D0 L1.2@S0/S0ix→D0 L0@S0/S0ix timing is shown in figure 3-10:

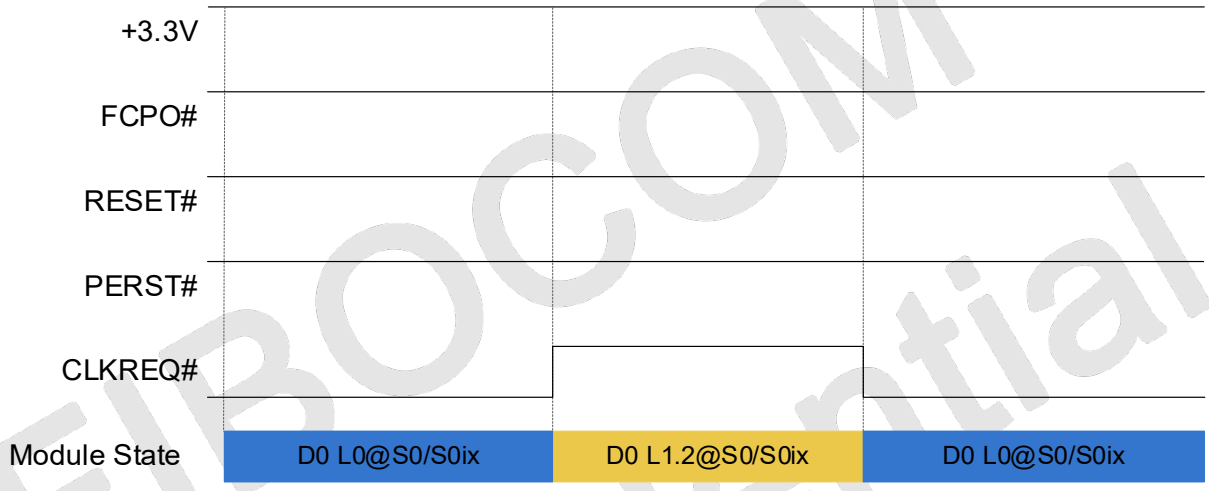


Figure 3-10 D0 L1.2 timi

**Note：**

When USB is used as data transfer interface in Chrome/Android/Linux OS, there is no PCIe link state. But when USB goes into suspend it also needs to follow the timing above (If PERST# and CLKREQ# are floating, don't control PERST# and CLKREQ#).

#### 3.3.4.2 $D3_{cold}$ L2

Module supports PCIe goes into $D3_{cold}$ L2 state in Win10 system. In $D3_{cold}$ L2 state, PCIe link can be woken up by both modem and host. The D0 L0@S0/S0ix→$D3_{cold}$ L2@S0/S0ix→D0 L0@S0/S0ix timing is shown in Figure 3-11 and Figure 3-12:

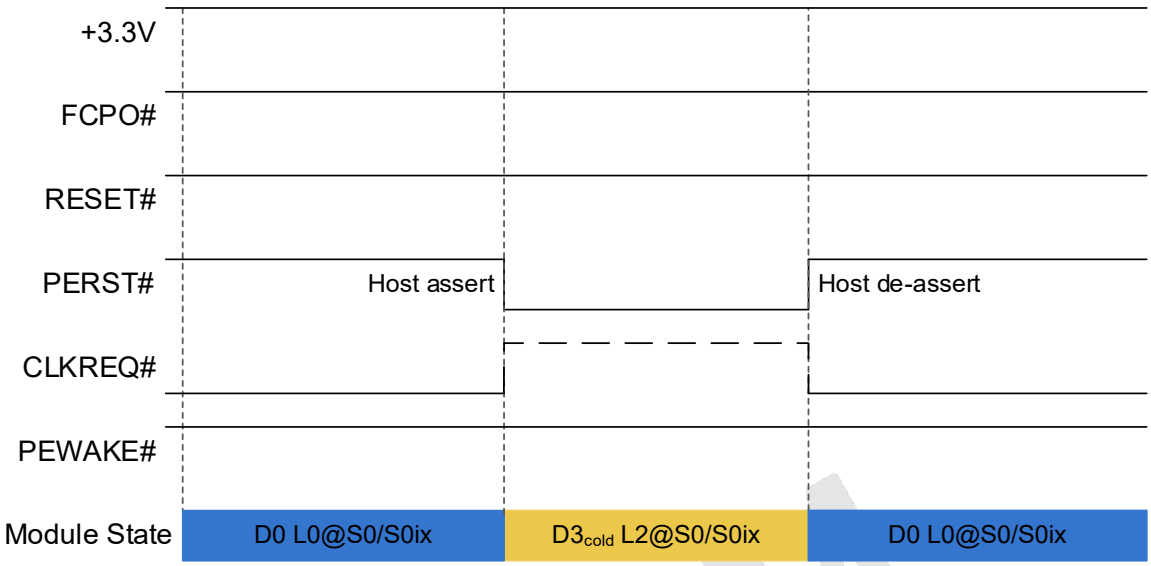


Figure 3-11 $D3_{cold}$ L2 timing (Host wakeup)

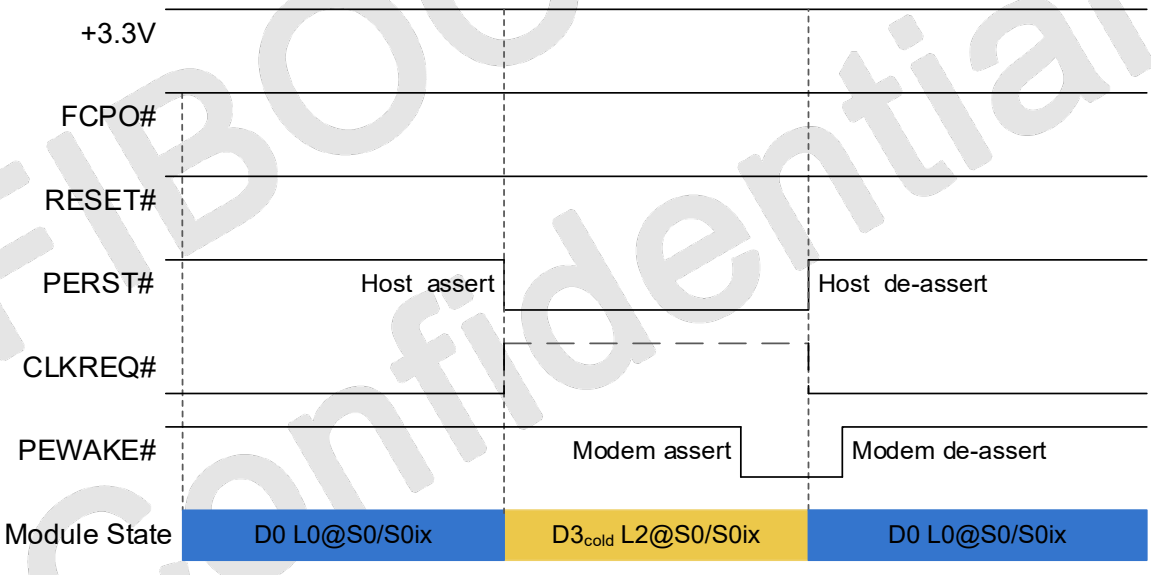


Figure 3-12 $D3_{cold}$ L2 timing (Modem wakeup)

**Note：**

When USB is used as data transfer interface in Chrome/Android/Linux OS, there is no PCIe link state, so don't need to follow timing above.

### 3.3.5 Timing Application

The recommended timing application in Win10 OS is as below table:

| System status | | Timing Application |
|---|---|---|
| S0ix (Modem standby) | D0 L1.2 | Refer to section 3.3.4.1 Figure 3-10 D0 L1.2 Timing |
| | $D3_{cold}$ L2 | Refer to section 3.3.4.2 Figure 3-11/3-12 $D3_{cold}$ L2 timing |
| S3, S4, S5 | Power on (back to S0) | Refer to section 3.3.1.2 Figure 3-5 Timing control for start-up |
| | Power off (out of S0) | Refer to section 3.3.2 Figure 3-6 Software power off timing |
| G3 boot | Power on | Refer to section 3.3.1.2 Figure 3-5 Timing control for start-up |
| Warm boot | | Refer to section 3.3.3 Figure 3-9 Reset timing 2nd |
| Modem FW upgrade / Modem recovery | | Refer to section 3.3.3 Figure 3-8 Reset timing 1st |

Intel X86 platforms must follow the table above. AMD X86 platforms should follow the table above and meet the special request of platform itself.

The recommended timing application in Chrome/Android/Linux OS is as below table:

| System status | Timing Application |
|---|---|
| Power on | Refer to section 3.3.1.2 Figure 3-5 Timing control for start-up |
| Shut down | Refer to section 3.3.2 Figure 3-6 Software power off timing |
| Connect standby | Refer to section 3.3.4.1 Figure 3-10 D0 L1.2 Timing |
| Restart | Refer to section 3.3.3 Figure 3-9 Reset timing 2nd |
| Modem FW upgrade / Modem recovery | Refer to section 3.3.3 Figure 3-8 Reset timing 1st |

## 3.4 IPC Interface

L850 module supports PCIe and USB interface for data request. PCIe & USB interface functions are as below table:

| Interface | System | Priority | Description |
|---|---|---|---|
| PCIe | Win10 | High | Priority: PCIe>USB<br>If PCIe and USB ports both connected with PC, module will initial PCIe first, then disable USB port |
| USB | Chrome OS /Android/Linux | Low | It must disconnect PCIe port, only keep USB connecting.<br>If keep PCIe and USB connecting both, it needs disable PCIe by BIOS/UEFI of PC |

### 3.4.1 PCIe Interface

L850 module supports PCIe Gen1 interface and one data transmission channel. BIOS configuration must follow X86 platform BKC (Best Know Configuration) reference design.

PCIe interface is initialized with host driver, and then mapped MBIM & GNSS port in Win10 OS. The MBIM interface is used for data transfer and GNSS port is used for receiving GNSS data.

#### 3.4.1.1 PCIe Interface Definition

| Pin# | Pin Name | I/O | Reset Value | Description | Type |
|---|---|---|---|---|---|
| 41 | PETn0 | O | - | PCIe TX differential signal Negative | - |
| 43 | PETP0 | O | - | PCIe TX differential signal Positive | - |
| 47 | PERn0 | I | - | PCIe RX differential signal Negative | - |
| 49 | PERP0 | I | - | PCIe RX differential signal Positive | - |
| 53 | REFCLKN | I | - | PCIe reference clock signal Negative | - |
| 55 | REFCLKP | I | - | PCIe reference clock signal Positive | - |
| 50 | PERST# | I | PU | Asserted to reset module PCIe interface default. If module went into coredump, it will reset whole module, not only PCIe interface. Active low, internal pull up(10KΩ) | 3.3V |
| 52 | CLKREQ# | I/O | PU | Asserted by device to request a PCIe reference clock be available (active clock state) in order to transmit data. It also used by L1 PM Sub states mechanism, asserted by either host or device to initiate an L1 exit. Active low, internal pull up(10KΩ) | 3.3V |
| 54 | PEWAKE# | O | L | Asserted to wake up system and reactivate PCIe link from L2 to L0, it depends on system whether supports wake up functionality. Active low, open drain output and should add external pull up (100KΩ) on platform | 3.3V |

### 3.4.1.2 PCIe Interface Application

The reference circuit is shown in Figure 3-13:

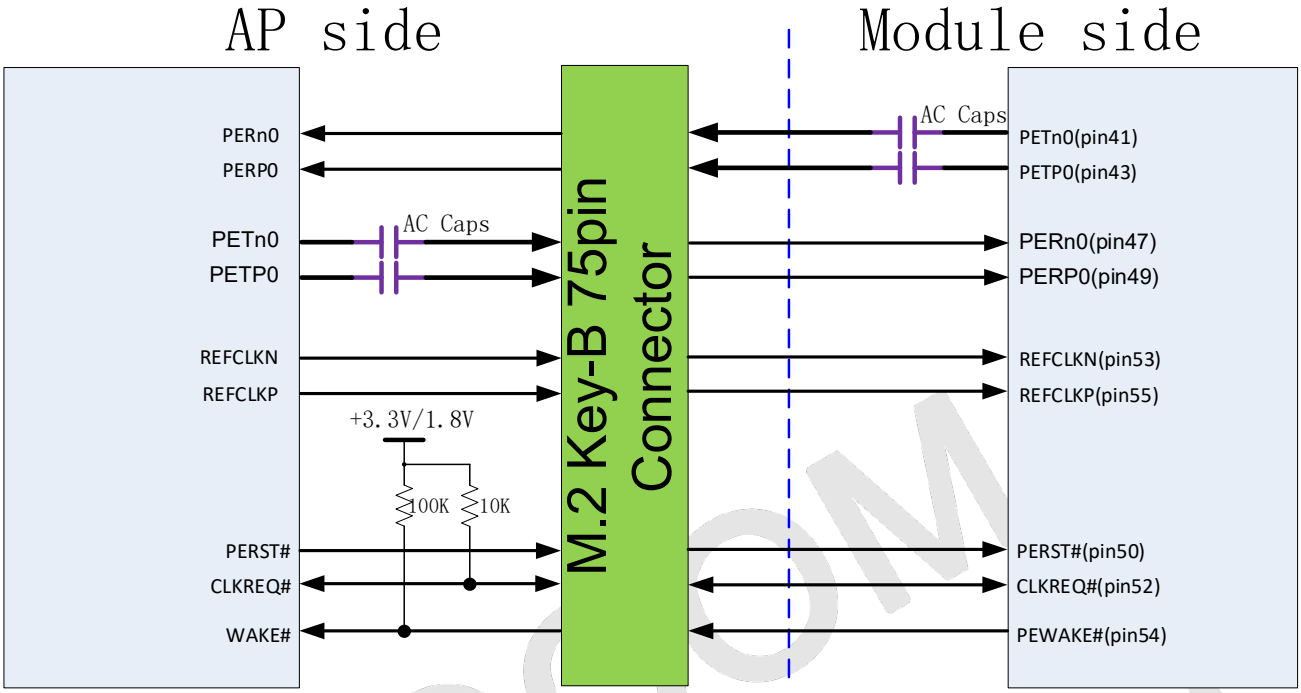


Figure 3-13 Reference circuit for PCIe interface

L850 module supports PCIe Gen1 interface, one lane. The PCIe interface including three differential pairs: transmit pair TXP/N, receiving pair RXP/N and clock pair CLKP/N.

PCIe can achieve the maximum transmission rate of 2.5 GT/s, and must strictly follow the rules below in PCB Layout:

- The differential signal pair lines should be parallel and equal in length;
- The differential signal pair lines should be short if possible and be controlled within 15 inch (380 mm) for AP end;
- The impedance of differential signal pair lines is recommended to be 100Ω, and can be controlled to 80~120Ω in accordance with PCIe protocol;
- Try to avoid the discontinuous reference ground, such as segment and space;
- When the differential signal lines go through different layers, the via hole of grounding signal should be in close to that of signal, and generally, each pair of signals require 1-3 grounding signal via holes and the lines should never cross the segment of plane;
- Try to avoid bended lines and avoid introducing common-mode noise in the system, which will influence the signal integrity and EMI of difference pair. As shown in Figure 3-14, the bending angle of all lines should be equal or greater than 135°, the spacing between difference pair lines should be larger than 20mil, and the line caused by bending should be greater than 1.5 times line width at least. When a serpentine line is used for length match with another line, the bended length of each segment

should be at least 3 times the line width (≥ 3W). The largest spacing between the bended part of the serpentine line and another one of the differential lines must be less than 2 times the spacing of normal differential lines (S1 < 2S);

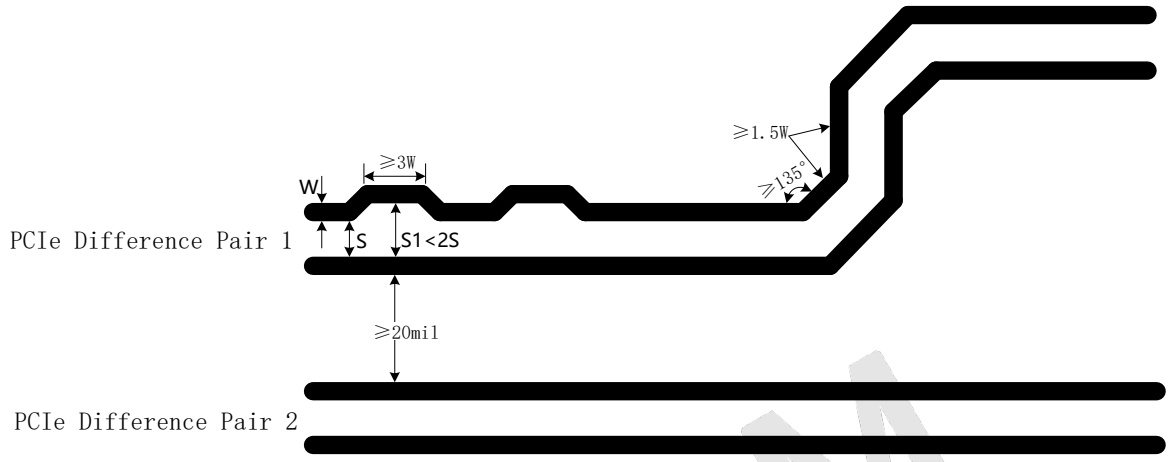


Figure 3-14 Requirement of PCIe line

- The difference in length of two data lines in difference pair should be within 5mil, and the length match is required for all parts. When the length match is conducted for the differential lines, the designed position of correct match should be close to that of incorrect match, as shown in Figure 3-15. However, there is no specific requirements for the length match of transmit pair and receiving pair, which means the length match is only required by intra differential pair rather than inter differential pair.

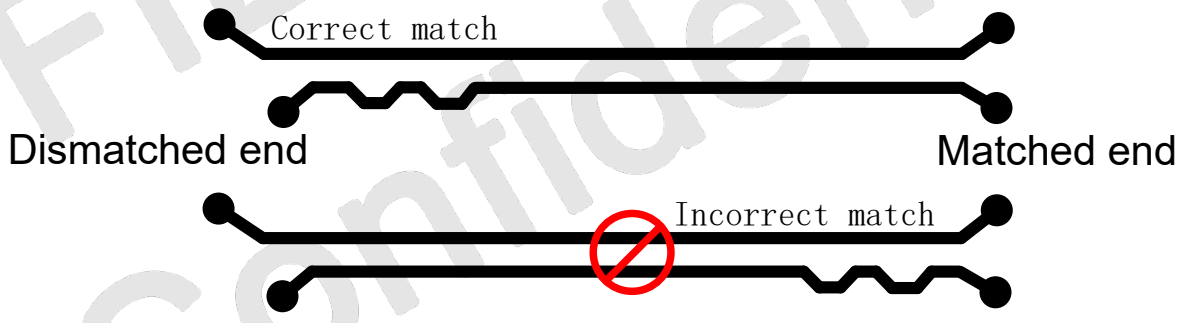


Figure 3-15 Length match design of PCIe difference pair

### 3.4.2 USB Interface

The L850 module supports USB2.0 which is compatible with USB High-Speed (480 Mbps) and USB Full-Speed (12 Mbps). It supports USB3.1 Gen1 using for LTE cat9 high speed data throughput at the same time. For the USB timing and electrical specification of L850 module, please refer to “Universal Serial Bus Specification 2.0” and “Universal Serial Bus Specification 3.0”.

USB interface initialized with host driver, and then mapped NCM and ACM ports in Chrome/Linux/Android OS. The NCM ports are used for data transfer. The ACM port is used for AT command. The port can be

configured in practical application.

### 3.4.2.1 USB Interface Definition

| Pin# | Pin Name | I/O | Description | Type |
|---|---|---|---|---|
| 7 | USB_D+ | I/O | USB data plus | 0.3---3V, USB2.0 |
| 9 | USB_D- | I/O | USB data minus | 0.3---3V, USB2.0 |
| 29 | USB3.0_TX- | O | USB3.0 transmit data minus | - |
| 31 | USB3.0_TX+ | O | USB3.0 transmit data plus | - |
| 35 | USB3.0_RX- | I | USB3.0 receive data minus | - |
| 37 | USB3.0_RX+ | I | USB3.0 receive data plus | - |

### 3.4.2.2 USB2.0 Interface Application

The reference circuit is shown in Figure 3-16:

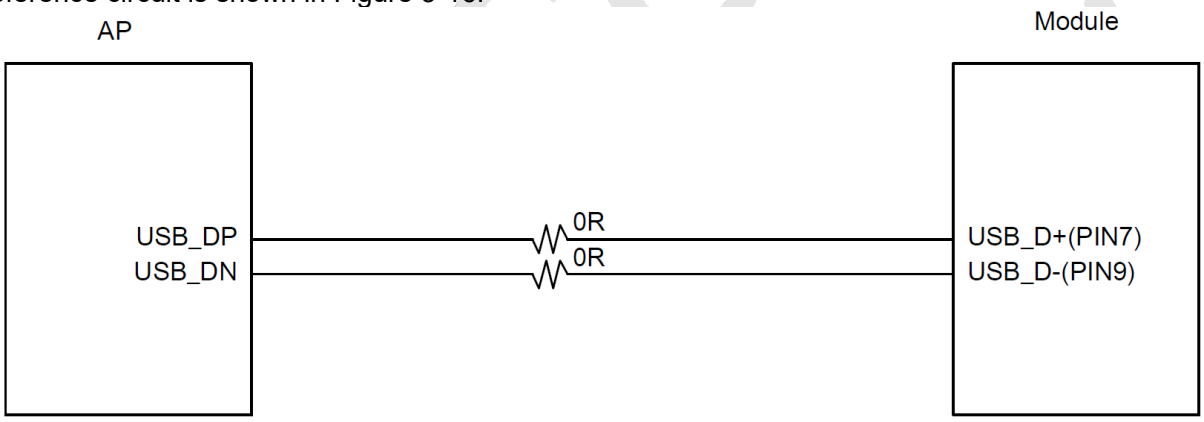


Figure 3-16 Reference circuit for USB 2.0 interface

USB_D- and USB_D+ are high speed differential signal lines with the maximum transfer rate of 480 Mbps, so the following rules should be followed carefully in the case of PCB layout:

- USB_D- and USB_D+ signal lines should have the differential impedance of 90Ω.
- USB_D- and USB_D+ signal lines should be parallel and have the equal length. The right angle routing should be avoided.
- USB_D- and USB_D+ signal lines should be routed on the layer that is adjacent to the ground layer, and wrapped with GND vertically and horizontally.

### 3.4.2.3 USB3.0 Interface Application

The reference circuit is shown in Figure 3-17:

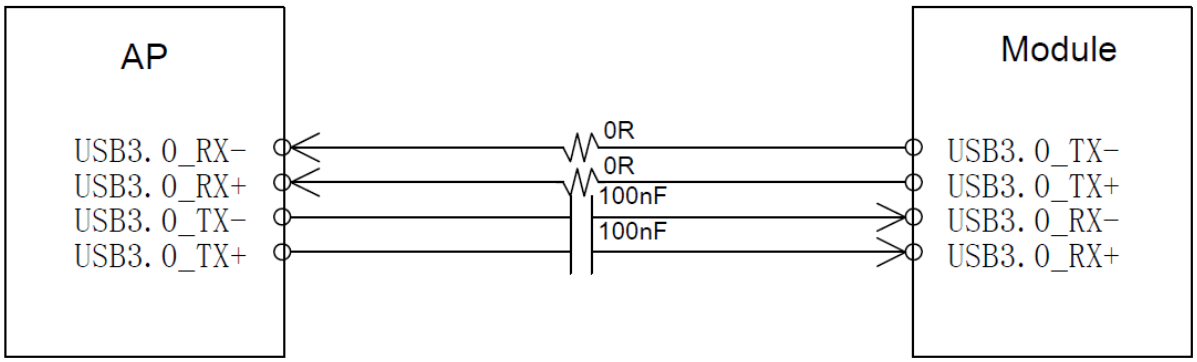


Figure 3-17 Reference circuit for USB3.0 interface

USB3.0 signals are super speed differential signal lines with the maximum transfer rate of 5 Gbps. So the following rules should be followed carefully in the case of PCB layout:

- USB3.0_TX-/USB3.0_TX+ and USB3.0_RX-/ USB3.0_RX+ are two pairs differential signal lines. The differential impedance should be controlled as 90Ω.
- The two pairs differential signal lines should be parallel and have the equal length. The right angle routing should be avoided.
- The two pairs differential signal lines should be routed on the layer that is adjacent to the ground layer, and wrapped with GND vertically and horizontally.

# 3.5 USIM Interface

The L850 module has a built-in USIM card interface, which supports 1.8V and 3V SIM cards.

## 3.5.1 USIM Pins

The USIM pins description is shown in the following table:

| Pin | Pin Name | I/O | Reset Value | Description | Type |
|---|---|---|---|---|---|
| 36 | UIM_PWR | PO | - | USIM power supply | 1.8V/3V |
| 30 | UIM_RESET | O | L | USIM reset | 1.8V/3V |
| 32 | UIM_CLK | O | L | USIM clock | 1.8V/3V |
| 34 | UIM_DATA | I/O | L | USIM data, internal pull up(4.7KΩ) | 1.8V/3V |
| 66 | SIM_DETECT | I | PD | USIM card detect, internal 390K pull-up.<br>Active high, and high level indicates SIM card is inserted; and low level indicates SIM card is detached. | 1.8V |

## 3.5.2 USIM Interface Circuit

### 3.5.2.1 N.C. SIM Card Slot

The reference circuit design for N.C. (Normally Closed) SIM card slot is shown in Figure 3-18:

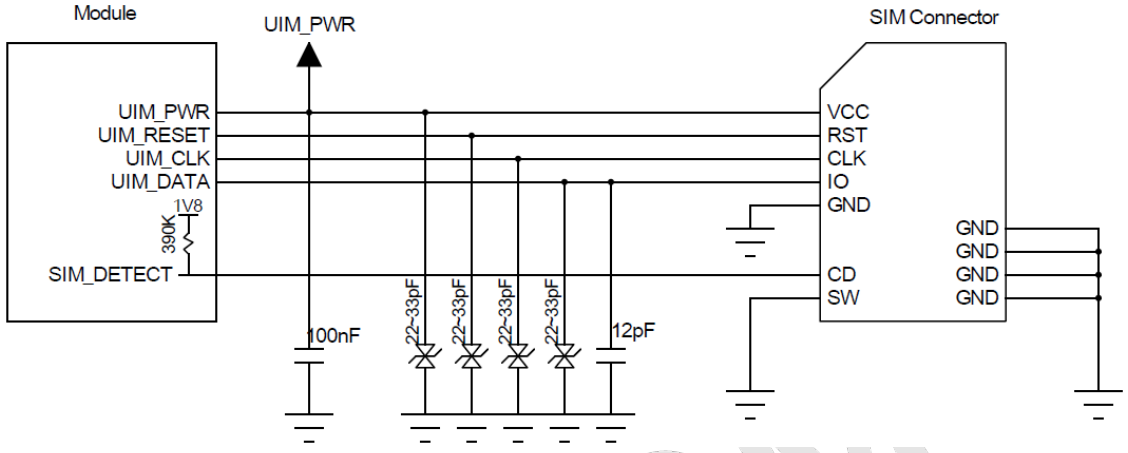


Figure 3-18 Reference circuit for N.C. SIM card slot

The principles of the N.C.SIM card slot are described as follows:

- When the SIM card is detached, it connects the short circuit between CD and SW pins, and drives the SIM_DETECT pin low.
- When the SIM card is inserted, it connects an open circuit between CD and SW pins, and drives the SIM_DETECT pin high.

### 3.5.2.2 N.O. SIM Card Slot

The reference circuit design for N.O. (Normally Open) SIM card slot is shown in Figure 3-19:

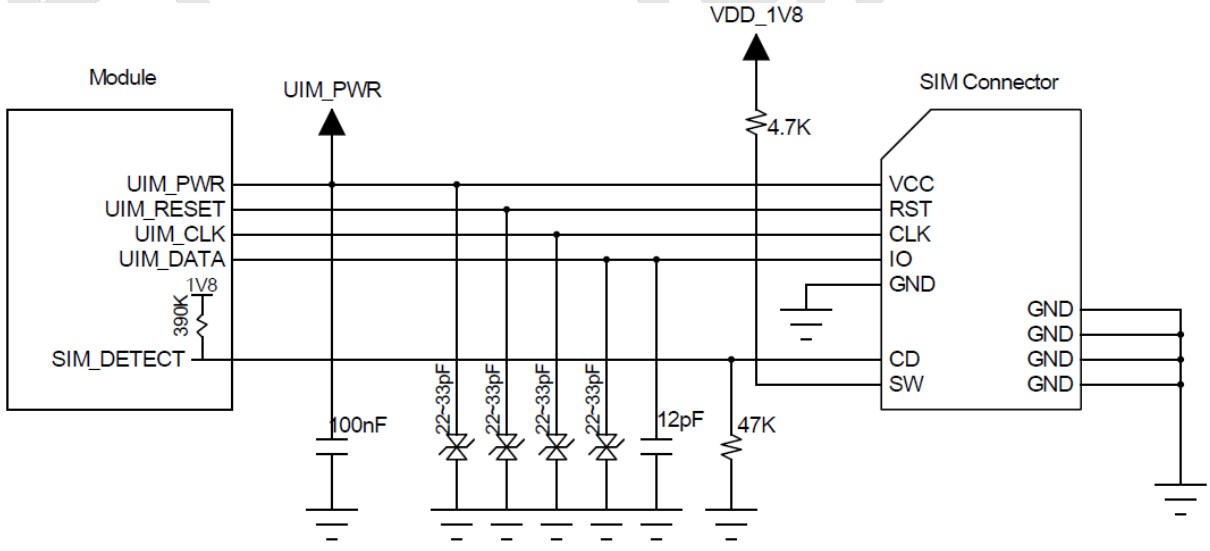


Figure 3-19 Reference circuit for N.O. SIM card slot

The principles of the N.O.SIM card slot are described as follows:

- When the SIM card is detached, it connects an open circuit between CD and SW pins, and drives the SIM_DETECT pin low.

- When the SIM card is inserted, it connects the short circuit between CD and SW pins, and drives the SIM_DETECT pin high.

### 3.5.3 USIM Hot-Plug

The L850 module supports the SIM card hot-plug function, which determines whether the SIM card is inserted or detached by detecting the SIM_DETECT pin state of the SIM card slot.

The SIM card hot-plug function can be configured by "AT+MSMPD" command, and the description for AT command is shown in the following table:

| AT Command | Hot-plug Detection | Function Description |
|---|---|---|
| AT+MSMPD=1 | Enable | Default value, the SIM card hot-plug detection function is enabled.<br>The module can detect whether the SIM card is inserted or not through the SIM_DETECT pin state. |
| AT+MSMPD=0 | Disable | The SIM card hot-plug detect function is disabled.<br>The module reads the SIM card when starting up, and the SIM_DETECT status will not be detected. |

After the SIM card hot-plug detection function is enabled, the module detects that the SIM card is inserted when the SIM_DETECT pin is high, then executes the initialization program and finish the network registration after reading the SIM card information. When the SIM_DETECT pin is low, the module determines that the SIM card is detached and does not read the SIM card.

**Note:**

SIM_DETECT is active high. It can be swapped to active low by AT CMD.

### 3.5.4 USIM Design

The SIM card circuit design should meet the EMC standards and ESD requirements with the improved capability to resist interference, to ensure that the SIM card can work stably. The following guidelines should be noted in design:

- The SIM card slot should be placed as close as possible to the module, and away from the RF antenna, DC/DC power supply, clock signal lines, and other strong interference sources.
- The SIM card slot with a metal shielding housing can improve the anti-interference ability.
- The trace length between the SIM card slot and the module should not exceed 100mm, or it could reduce the signal quality.
- The UIM_CLK and UIM_DATA signal lines should be isolated by GND to avoid crosstalk interference. If it is difficult for the layout, the whole SIM signal lines should be wrapped with GND as a group at

least.

- The filter capacitors and ESD devices for SIM card signals should be placed near to the SIM card slot, and the ESD devices with 22~33pF capacitance should be used.

# 3.6 Status Indicator

The L850 module provides three signals to indicate the operating status of the module, and the status indicator pins is shown in the following table:

| Pin | Pin Name | I/O | Reset Value | Pin Description | Type |
|---|---|---|---|---|---|
| 10 | LED1# | O | PD | System status LED, drain output. | 3.3V |
| 23 | WOWWAN# | O | PD | Module wakes up Host (AP)，Reserved | 1.8V |
| 48 | TX_BLANKING | O | PD | PA blanking output, external GPS control signal，Reserved | 1.8V |

## 3.6.1 LED#1 Signal

The LED#1 signal is used to indicate the operating status of the module, and the detailed description is shown in the following table:

| Module Status | LED1# Signal |
|---|---|
| RF function ON | Low level (LED On) |
| RF function OFF | High level (LED Off) |

The LED driving circuit is shown in Figure 3-20:

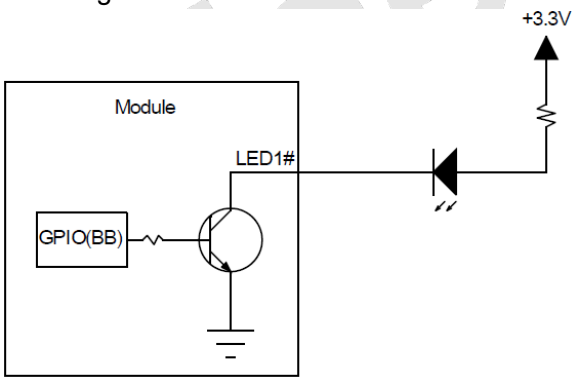


Figure 3-20 LED driving circuit

**Note:**

The resistance of LED current-limiting resistor is selected according to the driving voltage and the driving current.

## 3.7 Interrupt Control

The L850 module provides three interrupt signals, and the pin definition is as follows:

| Pin | Pin Name | I/O | Reset Value | Pin Description | Type |
|---|---|---|---|---|---|
| 8 | W_DISABLE1# | I | PD | Enable/Disable RF network | 3.3/1.8V |
| 25 | DPR | I | PU | BodySAR detection | 3.3/1.8V |
| 26 | W_DISABLE2# | I | PU | GNSS disable signal, Reserved | 3.3/1.8V |

### 3.7.1 W_DISABLE1#

The module provides a hardware pin to enable/disable WWAN RF function, and the function can also be controlled by the AT command. The module enters into flight mode after the RF function is disabled. The definition of W_DISABLE1# signal is as follows:

| W_DISABLE1# signal | Function |
|---|---|
| High/Floating | WWAN function is enabled, the module exits the flight mode. |
| Low | WWAN function is disabled, the module enters into flight mode. |

**Note：**

The function of W_DISABLE1# is enabled by default. It can be disabled by customer's request.

### 3.7.2 BODYSAR

The L850 module supports BodySAR function by detecting the DPR pin. The voltage level of DPR is high by default, and when the SAR sensor detects the closing human body, the DPR signal will be pulled down. As the result, the module then lowers down its emission power to its default threshold value, thus reducing the RF radiation on the human body. The threshold of emission power can be set by the AT Commands. The definition of DPR signal is shown in the following table:

| DPR signal | Function |
|---|---|
| High/Floating | The module keeps the default emission power |
| Low | Lower the maximum emission power to the threshold value of the module. |

## 3.8 Clock Interface

The L850 module supports a clock interface. It can output 26MHz clock.

| Pin | Pin Name | I/O | Reset Value | Pin Description | Type |
|---|---|---|---|---|---|
| 46 | SYSCLK | O | - | 26M clock output used for external audio codec and GNSS, etc., default disabled | 1.8V |

## 3.9 ANT Tunable Interface

The module supports ANT Tunable interfaces with two different control modes, i.e. MIPI interface and 3bit GPO interface. Through cooperating with external antenna adapter switch via ANT Tunable, it can flexibly configure the bands of LTE antenna to improve the antenna's working efficiency and save space for the antenna.

| Pin | Pin Name | I/O | Pin Description | Type |
|---|---|---|---|---|
| 56 | RFFE_SCLK | O | Tunable ANT control, MIPI Interface, RFFE clock | 1.8V |
| 58 | RFFE_SDATA | O | Tunable ANT control, MIPI Interface, RFFE data | 1.8V |
| 59 | ANTCTL0 | O | Tunable ANT control, GPO interface, bit0 | 1.8V |
| 61 | ANTCTL1 | O | Tunable ANT control, GPO interface, bit1 | 1.8V |
| 63 | ANTCTL2 | O | Tunable ANT control, GPO interface, bit2 | 1.8V |

**Note:**

The MIPI signal is limited to unidirectional function only.

## 3.10 Configuration Interface

The L850 module provides four pins to define WWAN-PCIe, USB3.1 type M.2 module:

| Pin | Pin Name | I/O | Reset Value | Pin Description | Type |
|---|---|---|---|---|---|
| 1 | CONFIG_3 | O | - | NC | - |
| 21 | CONFIG_0 | O | L | Internally connected to GND | - |
| 69 | CONFIG_1 | O | L | Internally connected to GND | - |
| 75 | CONFIG_2 | O | L | Internally connected to GND | - |

The M.2 module configuration is shown in the following table:

| Config_0 (pin21) | Config_1 (pin69) | Config_2 (pin75) | Config_3 (pin1) | Module Type and Main Host Interface | Port Configuration |
|---|---|---|---|---|---|
| GND | GND | GND | NC | WWAN–USB3.1 Gen1, PCIe Gen1 | 0 |

Please refer to “PCI Express M.2 Specification Rev1.2” for more details.

# 4 Radio Frequency

## 4.1 RF Interface

### 4.1.1 RF Interface Functionality

The L850 module supports two RF connectors used for external antenna connection. As the Figure 4-1 shows, “M” is for Main antenna, which is used to receive and transmit RF signal; “D/G” is for Diversity antenna, which is used to receive the diversity RF and GNSS signals.

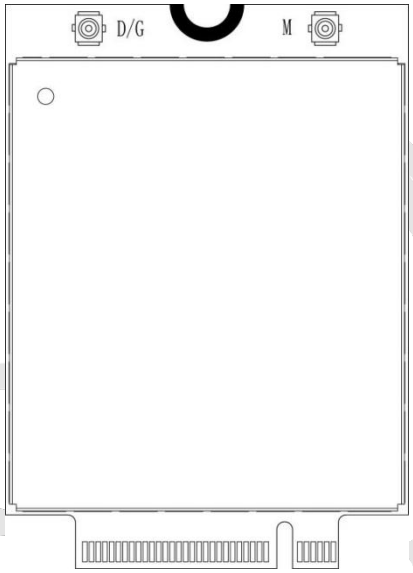


Figure 4-1 RF connectors

### 4.1.2 RF Connector Characteristic

| Rated Condition | | Environment Condition |
|---|---|---|
| Frequency Range | DC~6GHz | Temperature Range: –40°C~+85°C |
| Characteristic Impedance | 50Ω | |

### 4.1.3 RF Connector Dimension

L850 module uses standard M.2 RF connectors. The RF connector part number is 818004607 manufactured by ECT Corporation, and the size is 2×2×0.6mm. The connector dimension is shown as following picture:

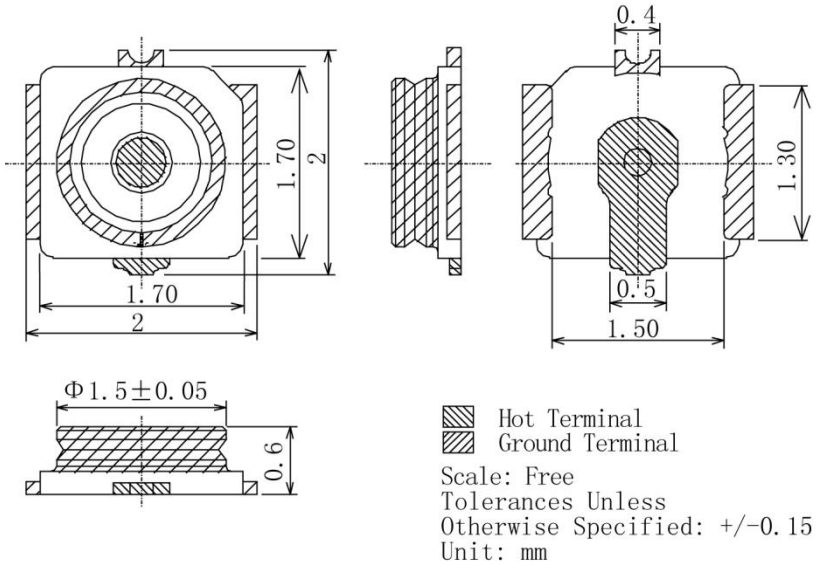


Figure 4-2 RF connector dimensions

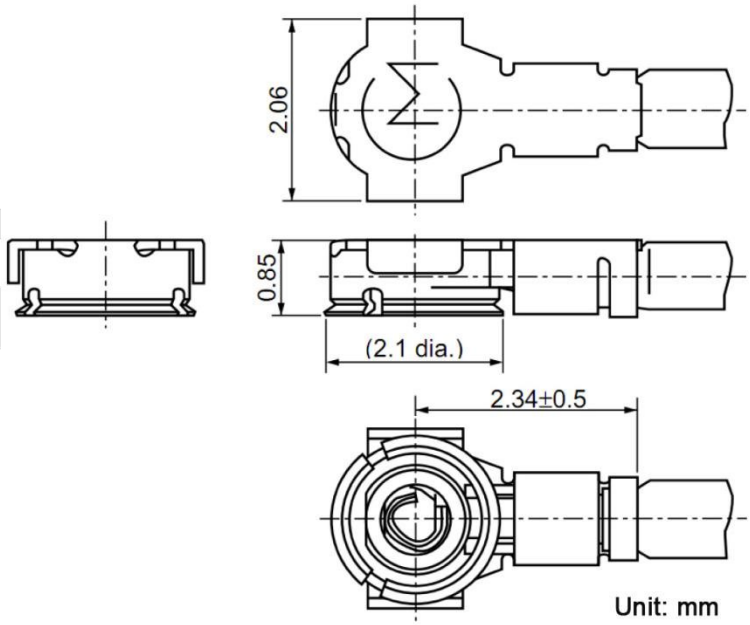


Figure 4-3 0.81mm coaxial antenna dimensions

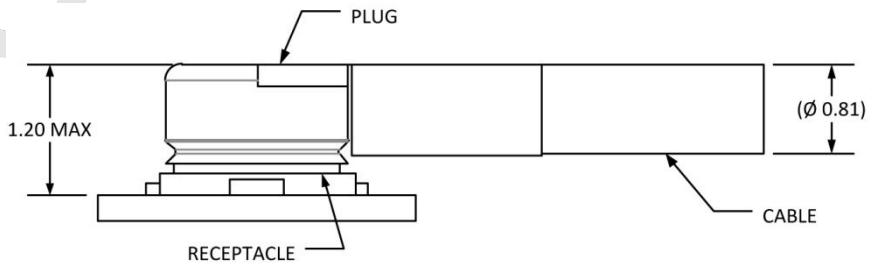


Figure 4-4 Schematic diagram of 0.81mm coaxial antenna connected to the RF connector

### 4.1.4 RF Connector Assembly

Mate RF connector parallel refer Figure 4-5, do not slant mate with strong force.

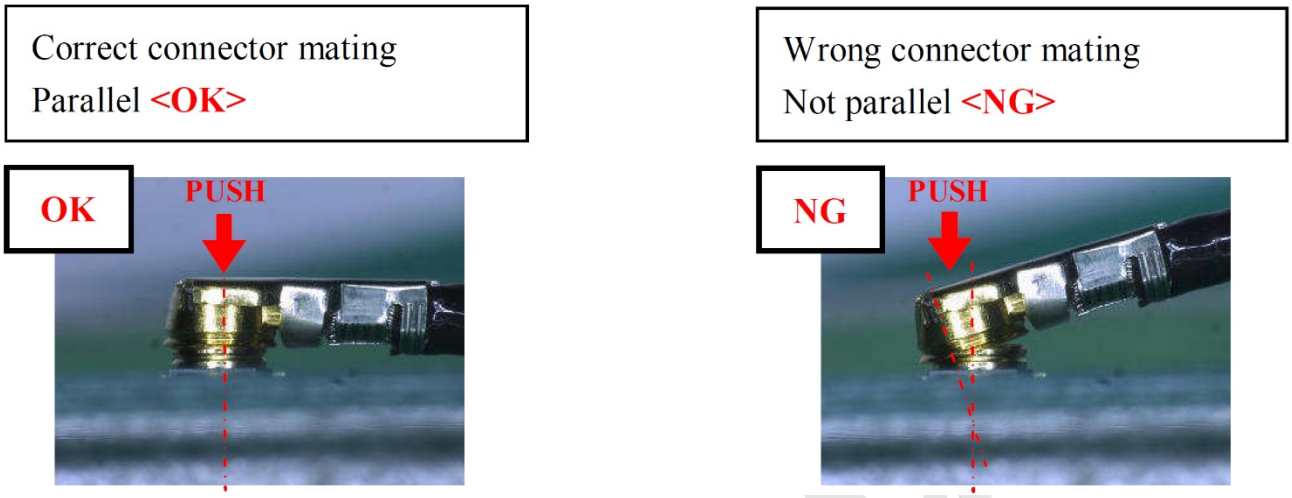


Figure 4-5 Mate RF connector

To avoid damage in RF connector unmating, it is recommended using pulling JIG as Figure 4-6, and the pulling JIG must be lifted up vertically to PCB surface (see Figure 4-7 and 4-8).

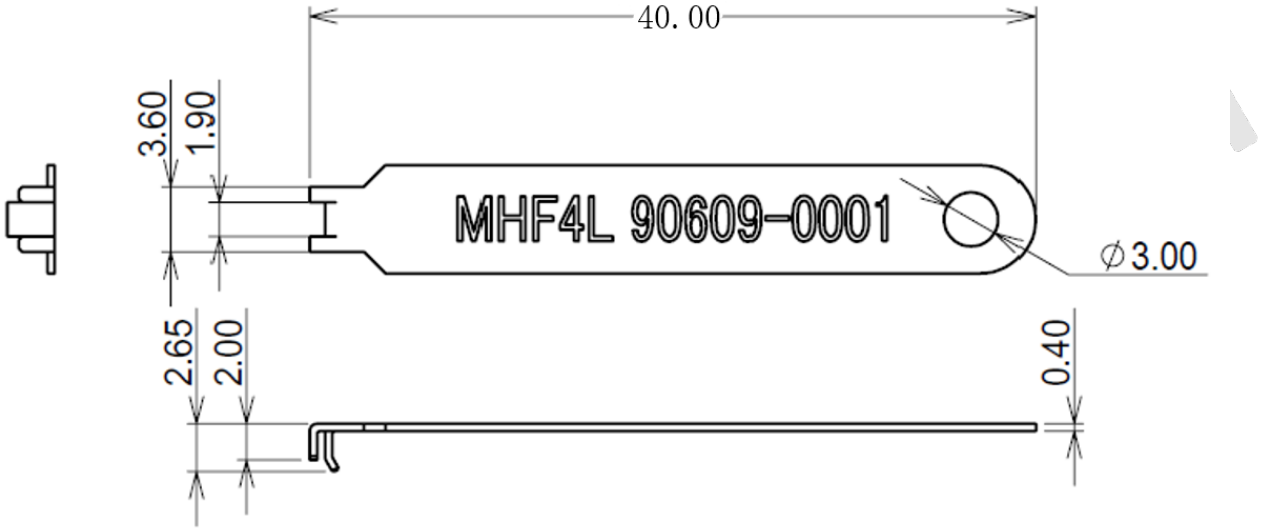


Figure 4-6 Pulling JIG

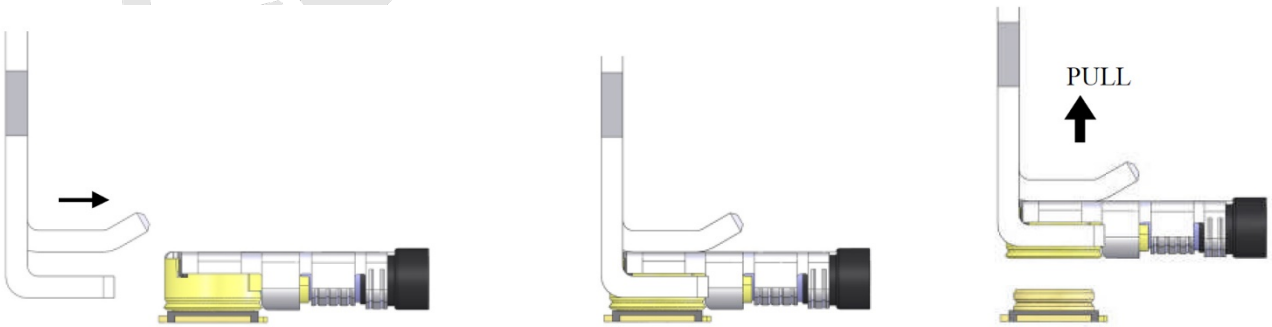


Figure 4-7 Lift up pulling JIG

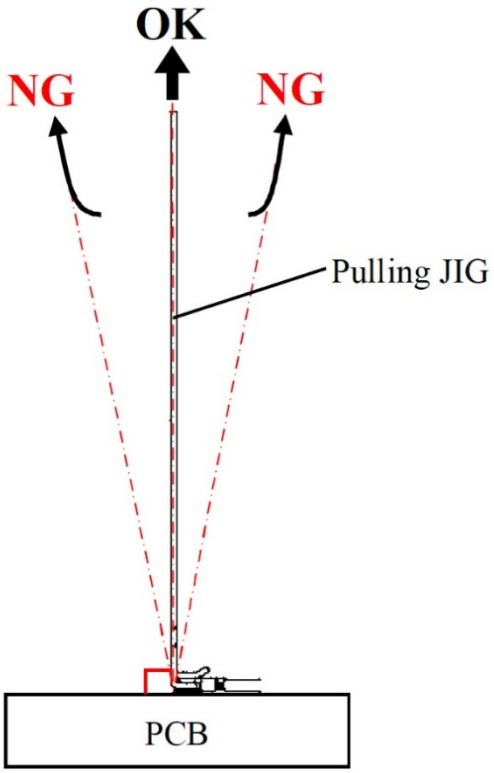


Figure 4-8 Pulling direction

## 4.2 Operating Band

The operating bands of L850 module are shown in the following table:

| Operating Band | Description | Mode | Tx (MHz) | Rx (MHz) |
|---|---|---|---|---|
| Band 1 | 2100MHz | LTE FDD/WCDMA | 1920 - 1980 | 2110 - 2170 |
| Band 2 | 1900MHz | LTE FDD/WCDMA | 1850 - 1910 | 1930 - 1990 |
| Band 3 | 1800MHz | LTE FDD | 1710 - 1785 | 1805 - 1880 |
| Band 4 | 1700MHz | LTE FDD/WCDMA | 1710 - 1755 | 2110 - 2155 |
| Band 5 | 850MHz | LTE FDD/WCDMA | 824 - 849 | 869 - 894 |
| Band 7 | 2600Mhz | LTE FDD | 2500 - 2570 | 2620 - 2690 |
| Band 8 | 900MHz | LTE FDD/WCDMA | 880 - 915 | 925 - 960 |
| Band 11 | 1500MHz | LTE FDD | 1427.9 - 1447.9 | 1475.9 - 1495.9 |
| Band 12 | 700MHz | LTE FDD | 699 - 716 | 729 - 746 |
| Band 13 | 700MHz | LTE FDD | 777 - 787 | 746 - 756 |
| Band 17 | 700MHz | LTE FDD | 704 - 716 | 734 - 746 |
| Band 18 | 800MHz | LTE FDD | 815 - 830 | 860 - 875 |
| Band 19 | 800MHz | LTE FDD | 830 - 845 | 875 - 890 |
| Band 20 | 800MHz | LTE FDD | 832 - 862 | 791 - 821 |
| Band 21 | 1500MHz | LTE FDD | 1447.9 - 1462.9 | 1495.9 - 1510.9 |
| Band 26 | 850MHz | LTE FDD | 814 - 849 | 859 - 894 |
| Band 28 | 700MHz | LTE FDD | 703 - 748 | 758 - 803 |
| Band 29 | 700MHz | LTE FDD | N/A | 716 - 728 |
| Band 30 | 2300MHz | LTE FDD | 2305 - 2315 | 2350 - 2360 |
| Band 66 | 1700MHz | LTE FDD | 1710 - 1780 | 2110 - 2200 |
| Band 38 | 2600MHz | LTE TDD | 2570 - 2620 | |
| Band 39 | 1900MHZ | LTE TDD | 1880 - 1920 | |
| Band 40 | 2300MHz | LTE TDD | 2300 - 2400 | |
| Band 41 | 2500MHZ | LTE TDD | 2496 - 2690 | |
| GPS L1 | - | - | - | 1575.42±1.023 |
| GLONASS L1 | - | - | - | 1602.5625±4 |
| BDS | - | - | - | 1561.098±2.046 |

## 4.3 Transmitting Power

The transmitting power for each band of L850 module is shown in the following table:

| Mode | Band | 3GPP Requirement (dBm) | Tx Power (dBm) | Note |
|---|---|---|---|---|
| WCDMA | Band 1 | 24+1.7/-3.7 | 23.5±1 | - |
| | Band 2 | 24+1.7/-3.7 | 23.5±1 | - |
| | Band 4 | 24+1.7/-3.7 | 23.5±1 | - |
| | Band 5 | 24+1.7/-3.7 | 23.5±1 | - |
| | Band 8 | 24+1.7/-3.7 | 23.5±1 | - |
| LTE FDD | Band 1 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 2 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 3 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 4 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 5 | 23±2.7 | 23+2/-1 | 10MHz Bandwidth, 1 RB |
| | Band 7 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 8 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 11 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 12 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 13 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 17 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 18 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 19 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 20 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 21 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 26 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 28 | 23+2.7/-3.2 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 30 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 66 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| LTE TDD | Band 38 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 39 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |

| Mode | Band | 3GPP Requirement (dBm) | Tx Power (dBm) | Note |
|---|---|---|---|---|
| | Band 40 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |
| | Band 41 | 23±2.7 | 23±1 | 10MHz Bandwidth, 1 RB |

**Note:**

Band 30 TX power range of L850-GL-03 serial module is between 22±1dBm, not 23±1dBm.

## 4.4 Receiver Sensitivity

The receiver sensitivity for each band of the L850 module is shown in the following table:

| Mode | Band | 3GPP Requirement (dBm) | Rx Sensitivity (dBm) Typical | Note |
|---|---|---|---|---|
| WCDMA | Band 1 | -106.7 | -109.5 | BER < 0.1% |
| | Band 2 | -104.7 | -110 | BER < 0.1% |
| | Band 4 | -106.7 | -109.5 | BER < 0.1% |
| | Band 5 | -104.7 | -111 | BER < 0.1% |
| | Band 8 | -103.7 | -110 | BER < 0.1% |
| LTE FDD | Band 1 | -96.3 | -101.5 | 10MHz Bandwidth |
| | Band 2 | -94.3 | -101.5 | 10MHz Bandwidth |
| | Band 3 | -93.3 | -101.5 | 10MHz Bandwidth |
| | Band 4 | -96.3 | -101.5 | 10MHz Bandwidth |
| | Band 5 | -94.3 | -102.5 | 10MHz Bandwidth |
| | Band 7 | -94.3 | -101 | 10MHz Bandwidth |
| | Band 8 | -93.3 | -102.5 | 10MHz Bandwidth |
| | Band 11 | -96.3 | -99 | 10MHz Bandwidth |
| | Band 12 | -93.3 | -100.5 | 10MHz Bandwidth |
| | Band 13 | -93.3 | -102.5 | 10MHz Bandwidth |
| | Band 17 | -93.3 | -102.5 | 10MHz Bandwidth |
| | Band 18 | -96.3 | -102.5 | 10MHz Bandwidth |
| | Band 19 | -96.3 | -103 | 10MHz Bandwidth |
| | Band 20 | -93.3 | -102.5 | 10MHz Bandwidth |
| | Band 21 | -96.3 | -99 | 10MHz Bandwidth |

| Mode | Band | 3GPP Requirement (dBm) | Rx Sensitivity (dBm) Typical | Note |
|---|---|---|---|---|
| | Band 26 | -93.8 | -103 | 10MHz Bandwidth |
| | Band 28 | -94.8 | -103 | 10MHz Bandwidth |
| | Band 29 | -93.3 | -101 | 10MHz Bandwidth |
| | Band 30 | -95.3 | -100.5 | 10MHz Bandwidth |
| | Band 66 | -95.8 | -101 | 10MHz Bandwidth |
| LTE TDD | Band 38 | -96.3 | -101 | 10MHz Bandwidth |
| | Band 39 | -96.3 | -101.5 | 10MHz Bandwidth |
| | Band 40 | -96.3 | -100.5 | 10MHz Bandwidth |
| | Band 41 | -94.3 | -100 | 10MHz Bandwidth |

**Note:**

The above values are measured for the dual antennas situation (Main+Diversity). For single main antenna (without Diversity), the sensitivity will drop around 3dBm for each band of LTE.

## 4.5 GNSS

L850 module supports GNSS with D/G antenna, including GPS/GLONASS/BDS. GNSS feature and performance are as below table.

| Description | Condition | Test Result | |
|---|---|---|---|
| | | MAX | Typical |
| Current | GPS fixing | 140mA@-130dBm | 120mA@-130dBm |
| | GPS tracking | 140mA@-130dBm | 120mA@-130dBm |
| | GPS Sleep | 3.5 mA@-130dBm | 2.0mA@-130dBm |
| TTFF | Cold start | 50s@-130dBm | 39s@-130dBm |
| | Warm start | 45s@-130dBm | 33s@-130dBm |
| | Hot Start | 3s@-130dBm | 2s@-130dBm |
| Sensitivity | Tracking | -156dBm | -160dBm |
| | Acquisition | -144dBm | -149dBm |

**Note:**

Please note that GNSS current is tested with RF disabled.

## 4.6 Antenna Design

The L850 module provides main and diversity antenna interfaces, and the antenna design requirements are shown in the following table:

| **L850 Module Main Antenna Requirements** | |
|---|---|
| Frequency range | The most proper antenna to adapt the frequencies should be used. |
| Bandwidth(WCDMA) | WCDMA band 1(2100): 250 MHz<br>WCDMA band 2(1900): 140 MHz<br>WCDMA band 4(1700): 445 MHz<br>WCDMA band 5(850): 70 MHz<br>WCDMA band 8(900): 80 MHz |
| Bandwidth(LTE) | LTE band 1(2100): 250 MHz<br>LTE band 2(1900): 140 MHz<br>LTE Band 3(1800): 170 MHz<br>LTE band 4(1700): 445 MHz<br>LTE band 5(850): 70 MHz<br>LTE band 7(2600): 190 MHz<br>LTE Band 8(900): 80 MHz<br>LTE Band 11(1500): 68 MHz<br>LTE Band 12(700): 47 MHz<br>LTE Band 13(700): 41 MHz<br>LTE Band 17(700): 42 MHz<br>LTE Band 18(800): 80 MHz<br>LTE Band 19(800): 80 MHz<br>LTE band 20(800): 71 MHz<br>LTE band 21(1500): 63 MHz<br>LTE band 26(850): 80 MHz<br>LTE band 28(700): 100 MHz<br>LTE band 29(700): 12 MHz<br>LTE band 30(2300): 55 MHz<br>LTE band 66(1700): 490 MHz<br>LTE band 38(2600): 50 MHz<br>LTE Band 39(1900): 40 MHz |

| L850 Module Main Antenna Requirements | |
|---|---|
| | LTE band 40(2300): 100 MHz<br>LTE band 41(2500): 194 MHz |
| Bandwidth(GNSS) | GPS: 2 MHz<br>GLONASS: 8 MHz<br>BDS: 4 MHz |
| Impedance | 50Ω |
| Input power | > 26dBm average power WCDMA & LTE |
| Recommended standing-wave ratio (SWR) | ≤ 2: 1 |

**Note:**

ANT on B30 suggestion: Peak gain < 0dBi, for FCC EIRP requirement, Efficient > 50% for carrier TRP requirement. If integrator doesn't follow the instruction, Fibocom doesn't take responsibility.

# 5 Structure Specification

## 5.1 Product Appearance

The product appearance for L850 module is shown in Figure5-1:

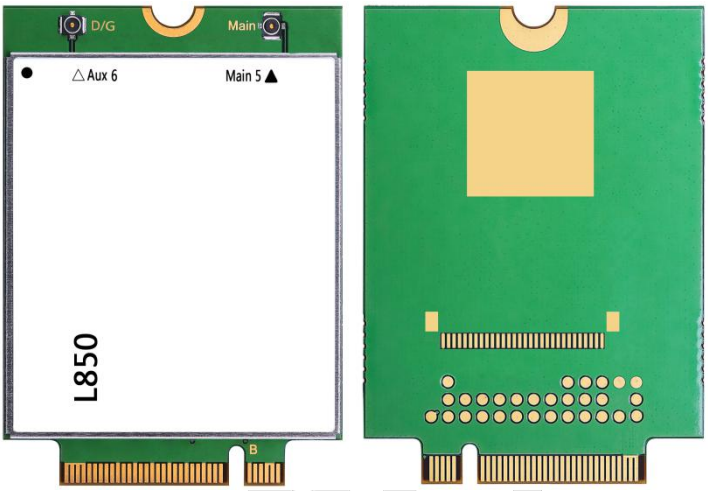


Figure 5-1 Module appearance

## 5.2 Dimension of Structure

The structural dimension of the L850 module is shown in Figure 5-2:

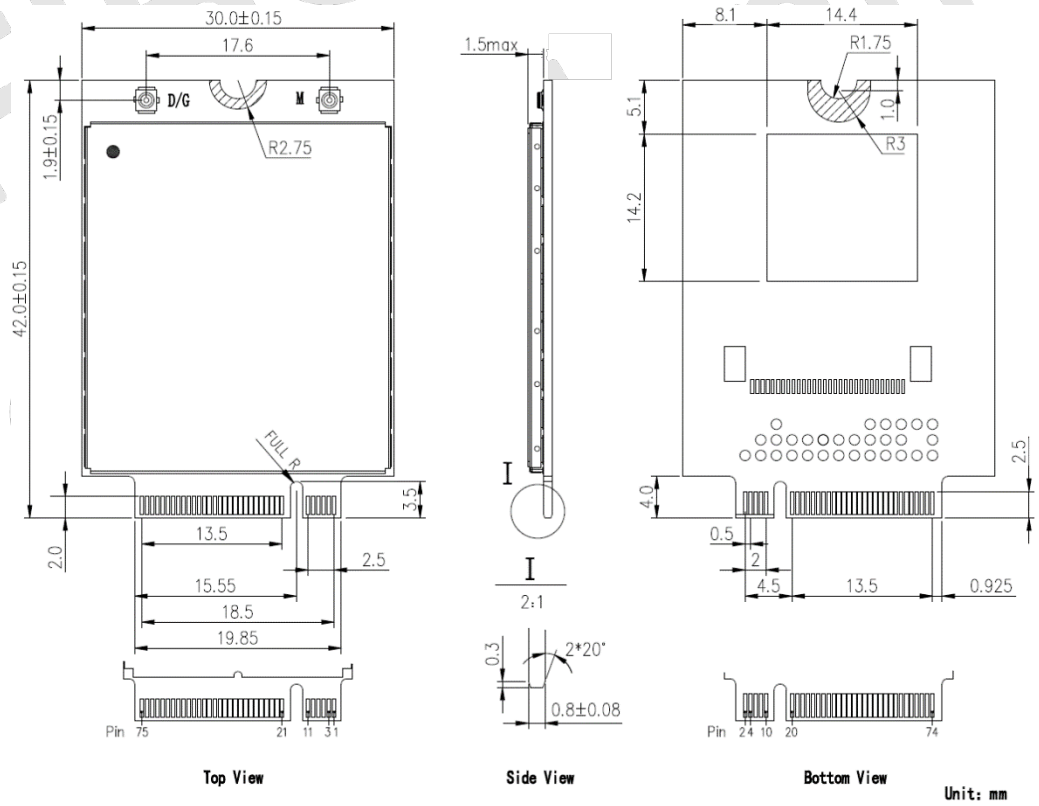


Figure 5-2 Dimension of structure

## 5.3 M.2 Interface Model

The L850 M.2 module adopts 75-pin gold finger as external interface, where 67 pins are signal pins and 8 pins are notch pins as shown in Figure 3-1. For module dimension, please refer to 5.2 Dimension of Structure. Based on the M.2 interface definition, L850 module adopts Type 3042-S3-B interface (30x42mm, the component maximum height on t top layer is 1.5mm, PCB thickness is 0.8mm, and KEY ID is B).

**Module Nomenclature**
**Sample type 3042-S3-B**

Type XX XX - XX - X - X[1]

| Width (mm) |
|---|
| 12 |
| 16 |
| 22 |
| 30 |

| Length (mm) |
|---|
| 16 |
| 26 |
| 30 |
| 38 |
| 42 |
| 60 |
| 80 |
| 110 |

| | Component Max Ht (mm) | |
|---|---|---|
| | Top Max[1] | Bottom Max[1] |
| S1 | 1.2 | 0**** |
| S2 | 1.35 | 0**** |
| S3 | 1.5 | 0**** |
| D1 | 1.2 | 1.35 |
| D2 | 1.35 | 1.35 |
| D3 | 1.5 | 1.35 |
| D4 | 1.5 | 0.7 |
| D5 | 1.5 | 1.5 |

| Key ID | Pin | Interface |
|---|---|---|
| A | 8-15 | 2x PCIe x1 / USB 2.0 / I2C / DP x4 |
| B | 12-19 | PCIe x2/SATA/USB 2.0/USB 3.0/HSIC/SSIC/Audio/UIM/I2C |
| C | 16-23 | Reserved for Future Use |
| D | 20-27 | Reserved for Future Use |
| E | 24-31 | 2x PCIe x1 / USB 2.0 / I2C / SDIO / UART / PCM |
| F | 28-35 | Future Memory Interface (FMI) |
| G | 39-46 | Generic (Not used for M.2)*** |
| H | 43-50 | Reserved for Future Use |
| J | 47-54 | Reserved for Future Use |
| K | 51-58 | Reserved for Future Use |
| L | 55-62 | Reserved for Future Use |
| M | 59-66 | PCIe x4 / SATA |

[1] Use ONLY when a double slot is being specified
[2] Label included in height dimension
[3] Key G is intended for custom use. Devices with this key will not be M.2-compliant. Use at your own risk!
[4] Insulating label allowed on connector-based designs

Figure 5-3 M.2 interface model

## 5.4 M.2 Connector

L850 module connects with host by M.2 connector which is built in host. The recommended part number is APCI0026-P001A manufactured by LOTES Corporation, and the dimensions is shown in Figure 5-4. The package of connector, please refer to the specification.

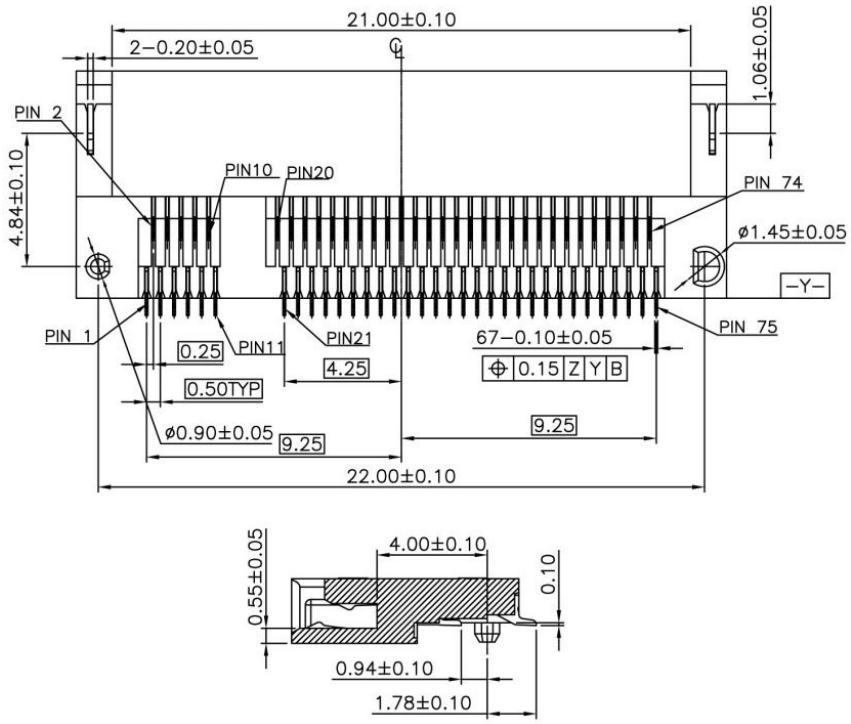


Figure 5-4 M.2 dimension of structure

# 5.5 Storage

## 5.5.1 Storage Life

Storage Conditions (recommended): Temperature is 23 ± 5°C, relative humidity is less than RH 60%.

Storage period: Under the recommended storage conditions, the storage life is 12 months.

# 5.6 Packing

The L850 module uses the tray sealed packing, combined with the outer packing method using the hard cartoon box, so that the storage, transportation and the usage of modules can be protected to the greatest extent.

**Note：**

The module is a precision electronic product, and may suffer permanent damage if no correct electrostatic protection measures are taken.

## 5.6.1 Tray Package

L850-GL-01 serial module uses tray package, 20 pcs are packed in each tray, with 5 trays including one empty tray on top in each box and 5 boxes in each case. Tray packaging process is shown in Figure 5-5:

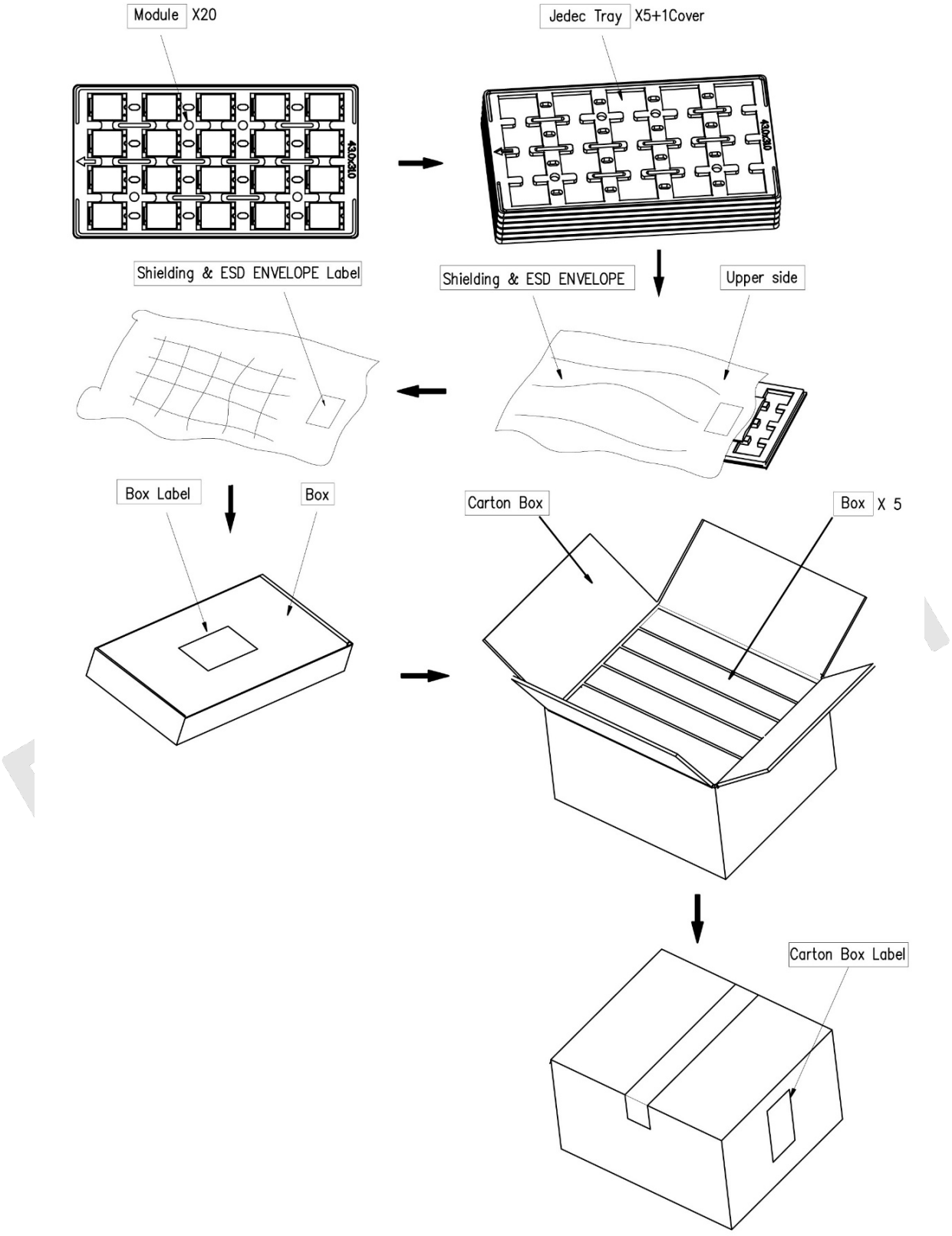


Figure 5-5 Tray packaging process

Other L850(except L850-GL-01 serial) module uses tray package, 20 pcs are packed in each tray, with 5 trays including one empty tray on top in each box and 6 boxes in each case. Tray packaging process is shown in Figure 5-6:

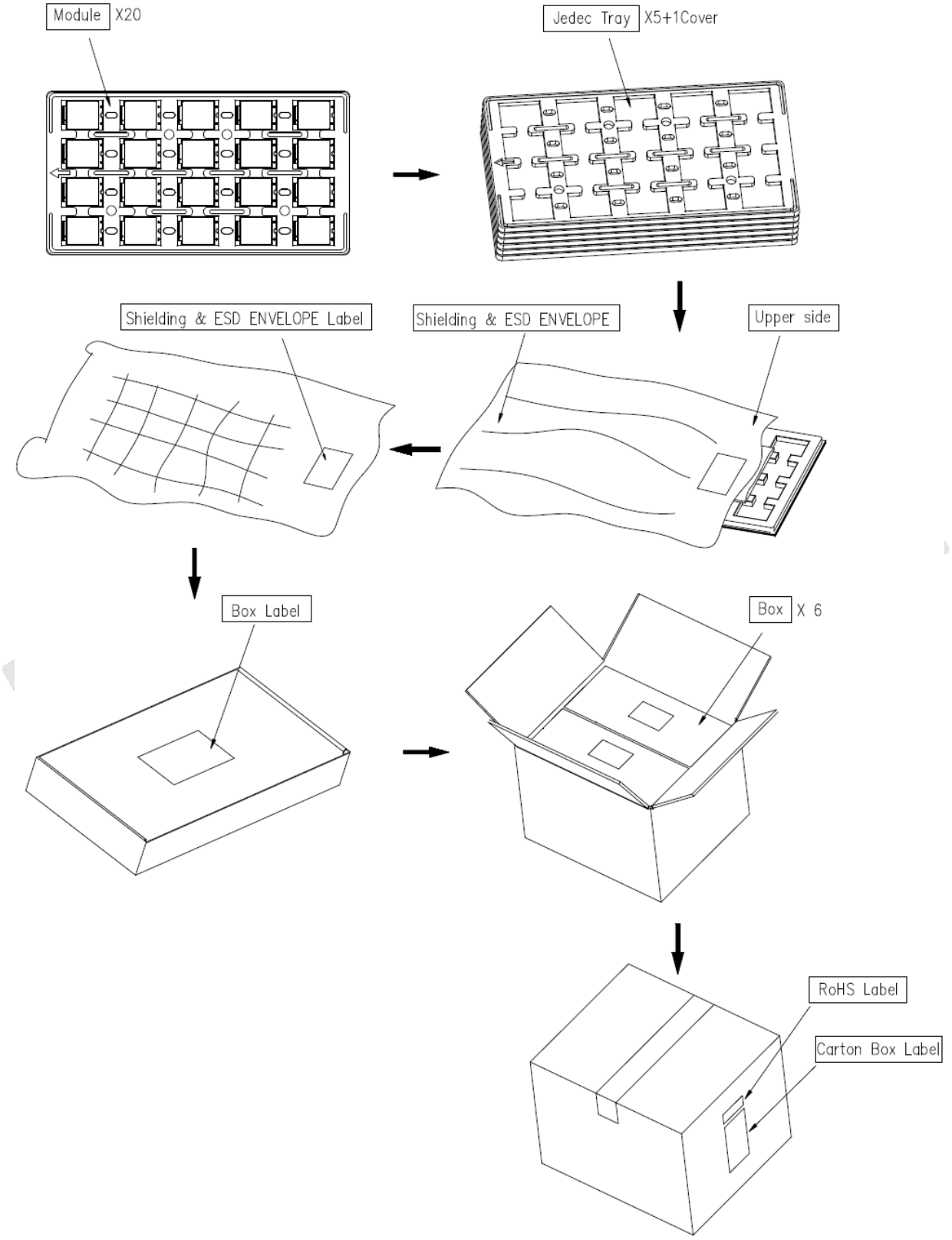


Figure 5-6 Tray packaging process

## 5.6.2 Tray Size

The pallet size of L850 module is 315×170×6.5mm, as shown in Figure 5-7:

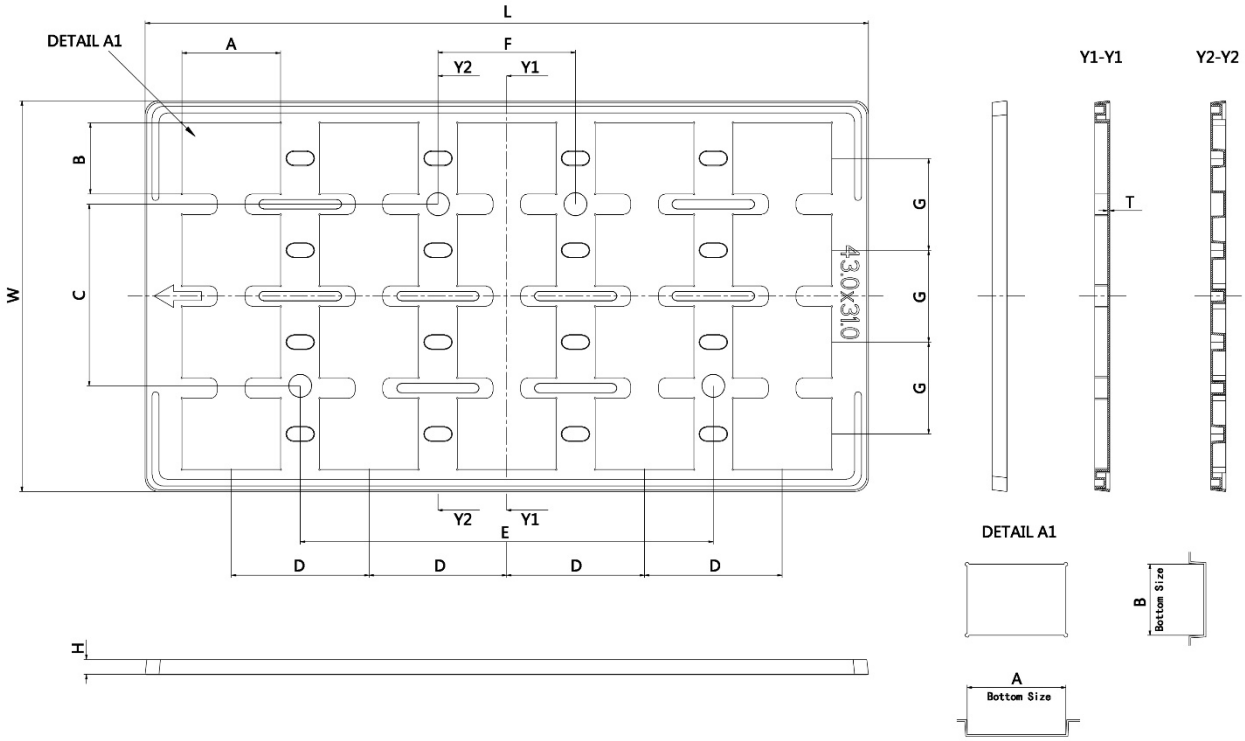


Figure 5-7 Tray size (unit: mm)

| ITEM | DIM (Unit: mm) |
|---|---|
| L | 315.0±2.0 |
| W | 170.0±2.0 |
| H | 6.5±0.3 |
| T | 0.8±0.1 |
| A | 43.0±0.3 |
| B | 31.0±0.3 |
| C | 79.0±0.2 |
| D | 60.0±0.2 |
| E | 180.0±0.2 |
| F | 60.0±0.2 |
| G | 40.0±0.2 |